A 20Gb/s 0.13um CMOS Serial Link

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1. Introduction

A 20Gb/s serial link in 0.13um CMOS has been designed. The output driver uses 2:1 output multiplexing with static phase offset calibration. A differential LC-PLL is used in the transmitter to reduce jitter and to achieve 10GHz on-chip oscillation frequency. The output driver clock capacitance is subsumed directly into the oscillator tank, thereby eliminating the static phase offset and power supply jitter associated with clock buffer chains. The receiver uses an 8:1 multiplexing ratio with a new latch structure. An on-chip 40-bit PRBS is used to verify correct data recovery. Total estimated power is 400mW for both transmitter and receiver; die area is 1.5mm x 1.5mm.

2. Motivation

Previous research in serial links has focused on transceivers that strive for the sweet spot across a number of design issues: high bandwidth, low power, low area[1],[2]. Such architectures, using clock multiplexing, are well suited for data rates around 5Gb/s(200ps/bit) but are questionable for higher data rates such as 20Gb/s(50ps/bit). At higher data rates, minimizing timing uncertainty becomes the primary concern. In conventional clock synthesis structures, such as in Figure 1, multiple phases are tapped off, buffered using tapered inverters, and finally used to multiplex data at the output pad, thereby compensating for the poor CMOS transconductance. However, the multi-phase voltage controlled oscillator, consisting of delay elements, exhibits unacceptable random jitter as well as static phase error due to parasitic and transistor mismatches between the multiple clock phases. Static phase error and random/power supply jitter are also increased by the buffer chains following the voltage controlled oscillator. In [1], eye closure due to static phase error is 15ps, insignificant for 4Gb/s, but relevant for 20Gb/s(50ps/bit). This eye closure is even more apparent in [3]. Mismatches, such as parasitic capacitance and transistor threshold mismatch, are expected to worsen with smaller transistor gate length and higher data rate.

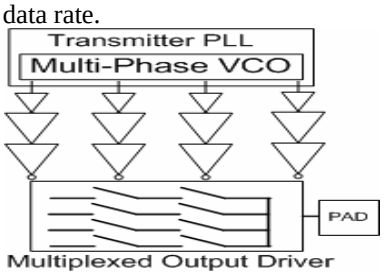

Figure 1: Conventional Multi-Phase Multiplexed Transmitter

3. 20Gb/s Transmitter Architecture

Figure 2 illustrates the block diagram of the proposed new architecture for a 20Gb/s serial link. This 20Gb/s transmitter uses a 2:1 output multiplexing stage, where the clocks come directly from the differential 10GHz LC Voltage Controlled Oscillator. The inductor used is a 150um x 150um differential symmetric square inductor, using thick M7 and M8, giving an inductance of 1.05nH, with an estimated Q=18 @ 10GHz. The symmetric inductor is placed across the terminals of back to back inverters,

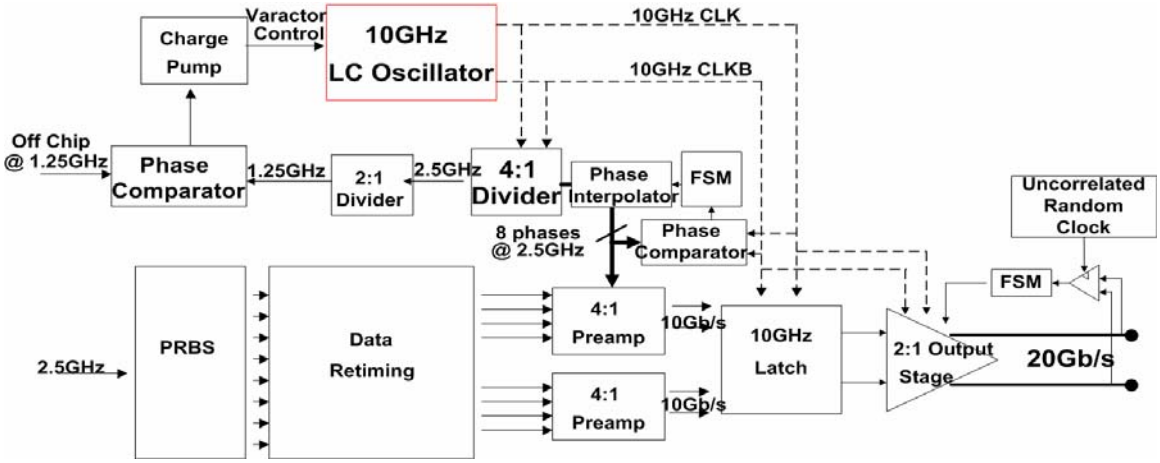

Figure 2: Transmitter Block Diagram

whose power supply is linearly regulated (Figure 3). Power supply regulation decreases power supply jitter into the LC tank as well as allowing for control of the transmitter output swing. The tank capacitance is modified by a coarse adjustment of digitally switched capacitance and a fine adjustment of inversion mode NMOS. Since the midpoint of the inductor acts like an AC ground, the effective tank inductance is only 0.5nH—at 10GHz resonance, the resonant capacitance is 500ff. Therefore, this architecture can resonate a significant amount of transistor loading capacitance and still exhibit large tuning range.

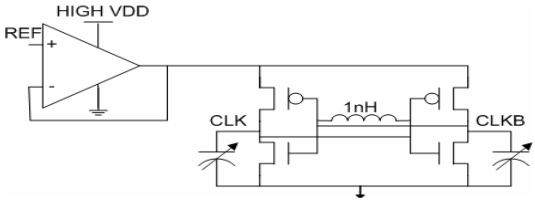

Figure 3: LC VCO with Power Supply Regulation

Although the 2:1 LC oscillator minimizes the random jitter as well as the static phase error mismatch, there may still exist residual static phase error, due to unbalanced parasitics, such as threshold mismatch in the final output driver. Such residual is calibrated using a calibration/reset phase, where a "1010" pattern is sent to the output, and sampled by an uncorrelated random clock[4]. Assuming random walk of the sampling clock, the number of hits will be uneven between asymmetric eyes. A switched capacitor bank at the tail node of the output driver affects the slew rate of the drivers, thereby correcting for uneven eye widths.

One potential difficulty is ensuring that the 10Gb/s data streams multiplexed from the multi-phased 2.5GHz 4:1 divider are in phase with the unadjustable 10GHz LC clock. This is solved by digitally using a phase comparator to find the zero crossings of the multi-phase clock. The phase comparator consists of a regenerative latch where the inputs are the 2.5GHz clock and the 10GHz clock, with the sampling point set by the 2.5GHz clock. The interpolator is then digitally adjusted such that the 10GHz latch closes the sampling window when the data is stable. Figure 4 shows the simulated HSPICE transmitter peak-peak jitter < 10ps and the simulated transmitter 100mV eye opening.

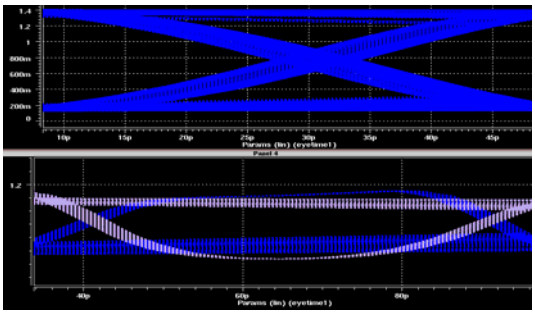

Figure 4: Transmitter Simulated Jitter and Transmitter Output Eye Diagram

4. 20Gb/s Receiver Architecture

Figure 5 shows the block diagram of the receiver. The receiver is an 8:1 demultiplexing front-end, consisting of an input track and hold followed by a regenerative latch. Here, the input sampling T/H samples with the 10GHz differential clock. However, the proceeding Strongarm regenerative latch is clocked by the

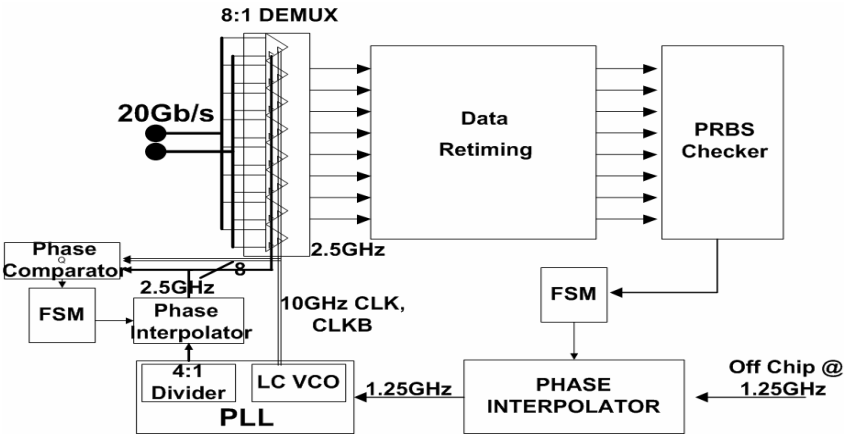

Figure 5: Receiver Block Diagram

2.5GHz clocks as well, allowing 400ps to convert to full digital level.

After the data is retimed into 8 streams of data @ 2.5GHz, a PRBS checker determines an approximate BER for the default static phase setting. From the BER value calculated, the phase interpolator is digitally switched to the next static phase setting, with a minimum step size of 5ps. The link is run until all all phases across the 50ps is swept, with the BER calculated for all ten phase settings. The phase setting exhibiting minimum BER is then statically set.

As in the transmitter, one crucial aspect of the design is phase alignment of the 10GHz clock with the 2.5GHz divided down clock. Again, a phase comparator running at 2.5GHz compares all eight phases with the 10GHz clock, and digitally sweeps the phase interpolator and sets the correct eight interpolated clocks.

The die is expected to tape-out in June 2002, using a 0.13um CMOS process. The expected die area is 1.5mm x 1.5mm, including transmitter, receiver, various PLL blocks comparing jitter, and test circuitry. Cascade Microtech probes will be used at the output pads of the transmitter and receiver, expecting relatively flat response up to 40GHz.

5. Conclusion

A 0.13um CMOS serial link transmitter and receiver has been designed and is currently in layout design. The transmitter uses a 2:1 output multiplexing, to reduce static phase error due to phase mismatch between multi-phase clock generators. Instead, a differential LC-VCO creates a 10GHz clock, thereby reducing power supply and random jitter, as well as static phase offset. A slow feedback loop corrects for residual static phase error, based upon statistical sampling with a random uncorrelated clock source. The receiver uses a similar LC-PLL structure, with the generated differential 10GHz clock source used for the input 8:1 demultiplexing receiver. Clock recovery is statically set by using a calibration phase to determine the optimum phase which achieves minimum BER.

6. Acknowledgments

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7. References

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