EE273 Digital Systems Engineering
Midterm Exam

February 12th, 2003

(Total time = 120 minutes, Total Points = 100)

Name: (please print)_____

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature:_____

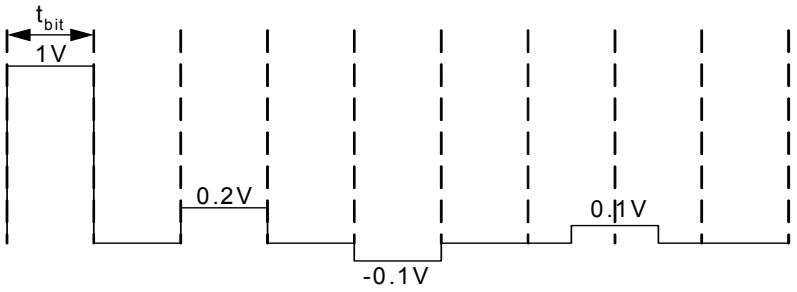
This examination is open notes open book. You may not, however collaborate in any manner on this exam. You have two hours to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary.

Before starting, please check to make sure that you have all 10 pages.

1		**30**
2		**15**
3		**25**
4		**10**
5		**20**
Total		**100**

Problem 1: Short Answer (30 Points: 10 questions, 3 points each)

A. Below is the impulse response of a single-ended bipolar signaling system – i.e. the response at the receiver given a bit-wide high input pulse at the transmitter. (a) What is the worst-case bit history if you want to send a high pulse, i.e. a "1"? (b) What is the worst-case bit history if you want to send a low pulse, i.e. a "0"? Each of the vertical dashed lines denotes a delay of t_{bit}.



a) When sending a high pulse "1" the worst case bit pattern is 1 X 0 X 1 X 0 0 X
b) When sending a high pulse "1" the worst case bit pattern is 0 X 1 X 0 X 0 0 X

Current bit ↑

B. What would be the proportional noise coefficient, Kn, that you would need to include due to intersymbol interference for the system above?

The noise that will be added is 0.2 + |-0.1| + 0.1 + 0.1 = 0.5 Volts

Swing is 1V – (-1V) = 2V ; Kn = 0.5/ 2 = 0.25

C. Consider a signaling system running at a data rate of 1GHz. After you've accounted for all of your bounded noise sources, you find that you have a net margin of 75mV. You externally add an additional 10 mV of RMS Gaussian noise to your system and measure a bit error rate of 1×10^{-3}. What is the BER of the native system (i.e. without the added Gaussian noise of 10mV RMS)? Probabilistically how long would you have had to run your system to empirically measure the native BER?

Vnm = 75mV ; let the initial gaussian noise be Vg; After adding 10mV of extra RMS gaussian noise, we get the net gaussian noise $Vgm' = (10^2 + Vgm^2)^{0.5}$
$V'snr = Vnm / Vgm' = 75 / (10^2 + Vgm^2)^{0.5}$; $BER' = \exp(-0.5 * V'snr^{2}) = 1 \times 10^{-3}$
⇨ Vgm = 17.5 mV
Native Vsnr = 75mV / 17.5mV = 4.28
Native BER = $\exp(-0.5 * Vsnr^2) = 1.05 \times 10^{-4}$

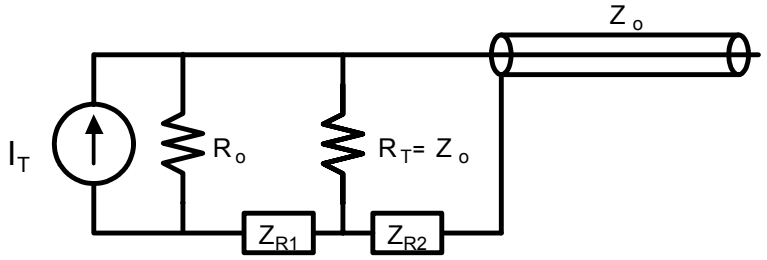
This implies we will have a bit error every $1 / 1.05 \times 10^{-4}$ clock cycles ie 9478 X 1ns = 9.5μs
(data rate of 1Gbps => one bit takes 1ns)

D. Consider a 4ns long circuit board trace with 80pF/m of capacitance that acts as a 50-Ω transmission line. You decide to run this trace on two different metal layers with a via between them. The via adds 10pF of capacitance at the center of the trace. How much does this increase the delay of the trace? What's the fastest rise time for which modeling this line as a lumped capacitance will give accurate results?

$Zo = (L/C)^{0.5} \Rightarrow L = Zo^2C = 50^2$ ohm* 80pF/m = 200 nH/m
Velocity , $v = (LC)^{-0.5} = 0.25 * 10^9$ m/s

Td = length / velocity => length of line = 4ns * v = 1meter
After adding a capacitor at the middle , C' = 90pF/m
New velocity , v'= 0.235 * 10^9 m/s
New delay Td' = 1meter/v' = 4.24ns
We should have rise time > 4 times the delay of half the line = 4 * 2.12 => Tr > 8.48ns

E. N signals are sharing a return path in the current-mode signaling system shown below. To reduce the amount of signal return crosstalk, the termination resistance has been pushed out past a portion of the return impedance, Z_{R1}, as shown below. In terms of the parameters shown below, what is the amount of transmitter signal return crosstalk, K_{XRT}, when the current source has a large but finite source resistance, Ro, as shown below?



Kxrt = Z_{R1} / (R_o + Z_o) + Z_{R2} / 2Z_o

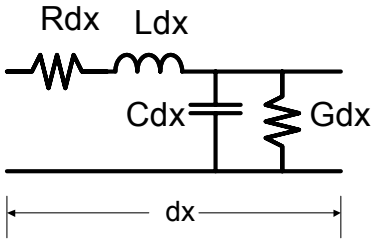
F. Consider a 4Gb/s signaling system. The attenuation of the 1 meter transmission line used by the system has an attenuation of 60% (A=0.6). There is essentially no attenuation at DC. If this line is used for bipolar differential signaling, what will the vertical eye opening be for the worst-case bit pattern? Express your answer as a fraction of signal swing.

Vertical eye opening = (2A –1) Vswing = 0.2 Vswing

G. Design a 2-tap filter (i.e. two drivers) that will equalize the line described in part G above.

Let the two taps of the filter be I_1 and I_2 .
When passing two dissimilar bits we use I_1 + I_2 = x(say)
When passing a series of "1"s or "0"s we use I_1 - I_2 = 0.6x (as attenuation is 0.6)
Let I_1 be 1.
Solving we get I_2 = 0.25

H. You are running a 100 kHz signal with a 1μs rise time across a 10 meter line with the infinitesimal wire model shown below: R=8 Ω/m, C=420pF/m, L=0.3μH/m, G=0. What components of R, L, G, and C would you use to model this line? What is the velocity of the signal traveling down the line?

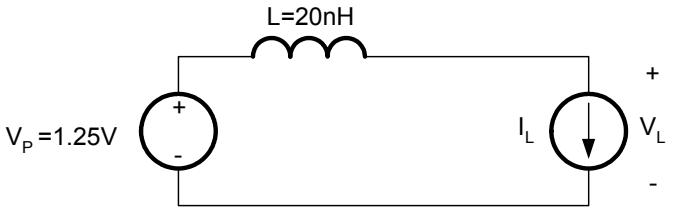


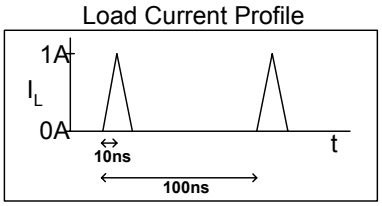
At 100 Khz , R >> ωL . Also the impedance presented by L = L/tr is small .
We can model this as RC line.
Delay of RC line = RC (or 0.69RC) = 80 * 4200pF = 3.36×10^{-7} sec
Velocity = length / delay = 29.76×10^{6} m/s

I. You decide to use the same line described above in part H to send a 1GHz signal with a rise time of 0.25ns. What components would you use to model this line? What is the velocity of the signal traveling down the line? If you terminate only the far end with a matched termination, what is the DC attenuation of the line?

At 1Ghz, R << ωL . So we can model as LC line..
Velocity = $(LC)^{0.5}$ = 28.17×10^{6} m/s
$Z_o = (L/C)^{0.5}$ = 26,7
DC Attenuated signal = $Z_o / Z_o +$ Rx = 26.7 / 26.7 + 80 = 0.25
=> DC attenuation = 0.75

J. Consider the following circuit. The supply lead has 20nH of inductance and the load current has the profile shown below. The supply, V_P, is 1.25V. Calculate the value of the bypass capacitor you would need to add in order to limit ripple on the 1.25V supply at the load, V_L, to ±10%. Assume the k factor is 1.





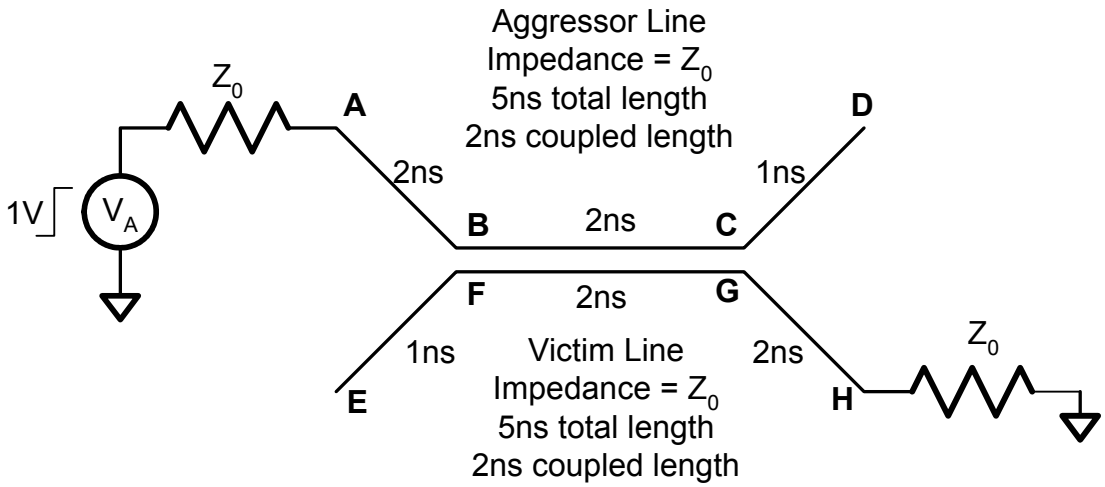
Iavg = (½ * 1A * 20ns) / 100 ns = 0.1 A
ΔV = 10% * 1.25 = 0.125V

Cb > L (Iav / ΔV)^2 + (Ki Iavg Tcycle)/ ΔV

Cb > 92.8 nF

Problem 2: Transmission Lines (15 Points)

Consider the pair of coupled transmission lines shown below. The two lines are in the center layer of a PC board (glass epoxy) surrounded by two ground planes above and below. The system designer chose to use source terminated lines to maximize the voltage swing but ran the signals in opposite directions. The coupled section of each line (BC and FG) has a capacitance to the other line of 30pF/m and 70pF/m to the shared ground planes. The aggressor line is driven by a 1V step source with a rise time of 100ps and a matched source impedance. The far end of the aggressor line is open. The victim line has its near end open and its far end terminated into a matched impedance. The delays of each line are as shown below.



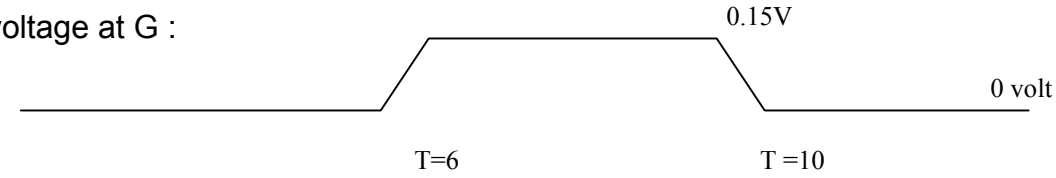
Using this information, sketch and dimension the voltage waveform at point G on the victim line. You may ignore any effects that lead to waves with less than 10mV amplitude.

Kcx = Cc / Cc + Cg = 30/ 100 = 0.3

This is a homogenous system . So Kfx =0 => kcx – klx =0 => Klx =Kcx

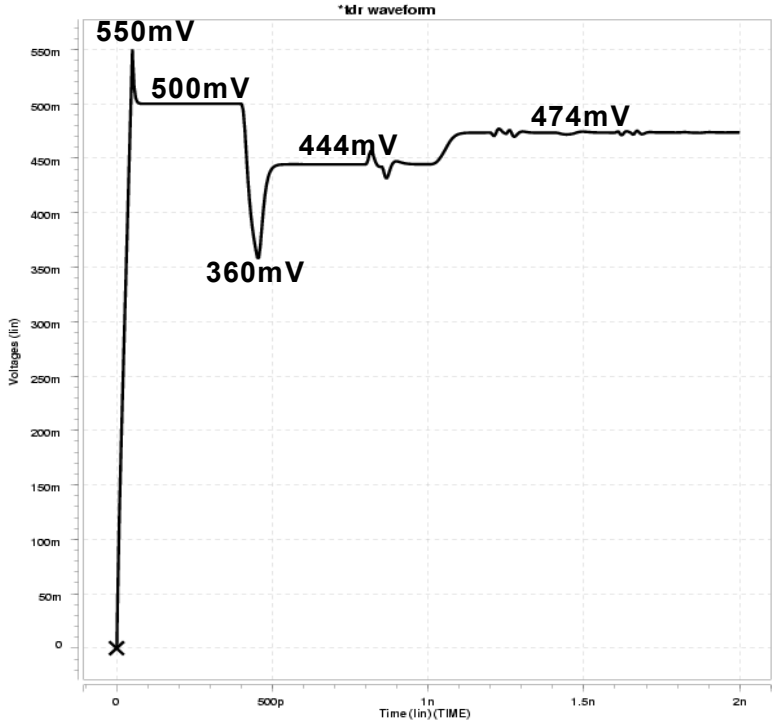
Krx = (kcx + klx)/ 4 = 0.15

voltage at G :

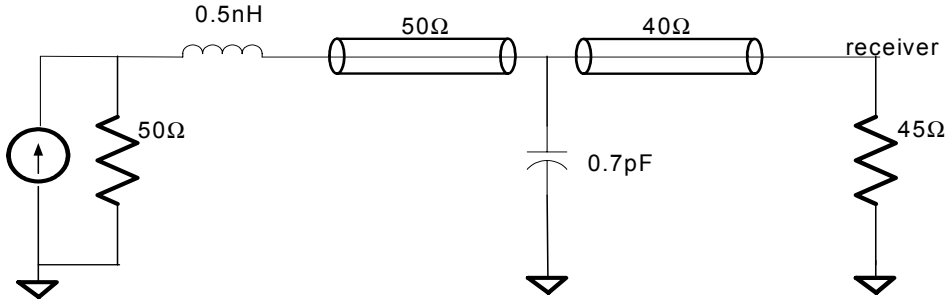


Problem 3: Signaling and Noise Analysis (25 points total)

Consider the TDR trace shown below of the worst-case signal line in your system. The interrogating signal is driven from a TDR with a 1V step, 50ps rise time, and a source resistance that is exactly 50-Ω. You may assume that the rise time of the interrogating edge is not degraded as it travels down the line.



(5 points) Sketch a line model for this transmission line labeling each of the components with their corresponding values.



First, you can see from the TDR that there are inductance and capacitance and two transmission lines.

i) Find the characteristic impedance, $Z = Zo\dfrac{V}{1-V}$

*50*0.5V/(1-0.5V)=50, 50*0.444 /(1-0.444) = 40, 50*0.474/(1-0.474) = 45*

ii) Calculate L value from $\tau = t_r \dfrac{\Delta V}{V} = 50ps\dfrac{50}{500} = 5ps = \dfrac{L}{50+50}$, *L = 0.5nH*

iii) Calculate R from $\tau = t_r \dfrac{\Delta V}{V} = 50ps\dfrac{140}{444} = 15.8ps = 50 \,||\, 40 * C$, *C =0.7pF*

A. (10 points) In the actual system, two of these lines will be used to send a bipolar differential signal. The driver for each line sends ±20mA of current with a tolerance of ±10% at 2Gb/s with a

100ps rise time. There is a matched source resistance with a tolerance of ±20%. The receiver has a combined sensitivity and offset voltage of ±10mV. What is the net margin (V_{NM}) and the margin ratio ($MR = V_{NM}/V_{GM}$) for this system?

This problem can be solved in two ways, either way can get the full credit
Find effective impedance value for each passive element, and find reflection coefficient from those

. *C(0.7pF) : |Z| =Δ t/C = 100ps/07pF = 143 Ω*
Effective terminal resistance : 143 || 40 = 31Ω
Reflection to the source direction : Kr = (50- 31)/(50+31) = 0.115
Reflection to rx direction : Kr = (40-143||50)/(40+143||50) = 0.04
R(45Ω) : Reflection to the source direction : Kr = (40-45)/(40+45) = 0.06

L(0.5nH): |Z| =L/Δ t = 0.5nH/100ps = 5 Ω
Effective source resistance : 5 + 50 = 55Ω
Reflection to the receiver direction : Kr = (50-55)/(50+55) = 0.05
*Total reflection is : Cap refl.*source refl. + Terminal refl*Source refl + Terminal refl*C refl*
*0.115*0.05 + 0.06*0.05 + 0.06*0.0.4 = 0.011*

You can calculate reflection form discontinuity by $Kr = \frac{\Delta V}{V} = \frac{\tau}{t_r}$

Reflection form the Capacitance : RC = 15.6ps, Kr=0.156
Reflection from the Inductance : L/R = 5ps, Kr = 0.05
Reflection from the terminal resistance : Kr = (40-45)/(40+45) = 0.06
*Total reflection is: Cap refl.*source refl. + Terminal refl*Source refl+ Terminal refl*C refl*
*0.156*0.05 + 0.06*0.05 + 0.06*0.156 = 0.02*

Assume we have Kn=0.02 from above,
The TDR graph shows when the source is 20mA step. Therefore voltage swing on the resistance is ±474mV as the grap. This system is using differential signaling. Voltage swing is doubled.
*Voltage swing : 474mV *2*2 = 1896 mV*
Discontinuity in Impedance : 0.02
*Current source mismatch : ±10% *948mV => 0.05*
*Source resistance mismatch : 10%*948mV => 0.05*
Kn = (0.05+0.05+0.02) = 0.12, knΔV = 227mV
Receiver offset : ±10m = ± 10mV
Bounded Noise: 237mV

V_{GM}: ΔV/2 = 948 mV
V_{NM}: 948mV – 237mV =711mV
Margin Ratio : 710/948 = 0.75
You can also think that voltage swing is 2V and there are noise from transmission line mismatch.

B. (5 points) You want to increase the bandwidth by using multi-level signaling. What is the maximum number of bits you could send every period assuming the clock is fixed at 1GHz?

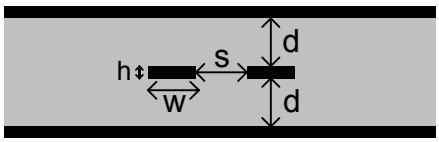
*ΔV =(N-1)*Vn*2 , 1896 = (N-1)*237mV*2 N=5.0 (N is number of signal level)*
$N = 2^b$, b=2 bits

C. (5 points) You find that your system has 10mV of RMS Gaussian noise. If you are running your system with the number of levels you found in part C, what is the bit error rate, BER, of your system?

*4 level signaling, V_{GM} = ΔV/2*1/3 = 316mV*
*BER = exp(-1/2 * ((316-237)/10)^2) = 2.8e-14*

Problem 4: Wire Modeling (10 Points Total)

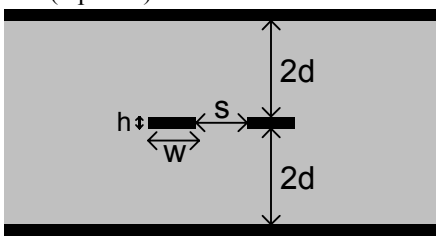
Consider two circuit board traces surrounded by two ground planes as shown below. The gray area is glass epoxy and the black areas are copper. The baseline case has the following parameters shown in the table below:



Description	Symbol	Value
Mutual Inductance	M	M_1
Self Inductance	L	L_1
Capacitance to Ground Planes	C_c	C_{c1}
Mutual Capacitance	C_m	C_{m1}
Resistance	R	R_1
Impedance	Z_o	Z_{o1}
Even-mode Impedance	Z_{even}	Z_{even1}
Odd-mode Impedance	Z_{odd}	Z_{odd1}
Velocity	V	v_1

To first approximation what are the new values for M, L, C_c, C_m, R, Z_o, Z_{even}, Z_{odd}, and v for the following cases? Give your answers in terms of the baseline values M_1, L_1, C_{c1}, C_{m1}, R_1, and Z_{o1}. You may ignore fringing effects.

A. (5 points) Case 1:



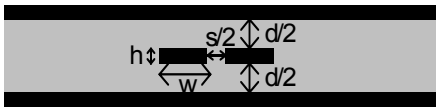
$M = M_1$
$L = 2\ L_1$
$C_c = 1/2\ C_c$
$Cm = Cm_1$
$R = R_1$
$Z_0 = 2\ Z_0$

$$Z_{even} = \sqrt{\frac{2L_1 + M_1}{1/2Cc_1}}$$

$$Z_{odd} = \sqrt{\frac{2L_1 - M_1}{1/2C_{c1} + 2C_{m1}}}$$

$V = V_1$

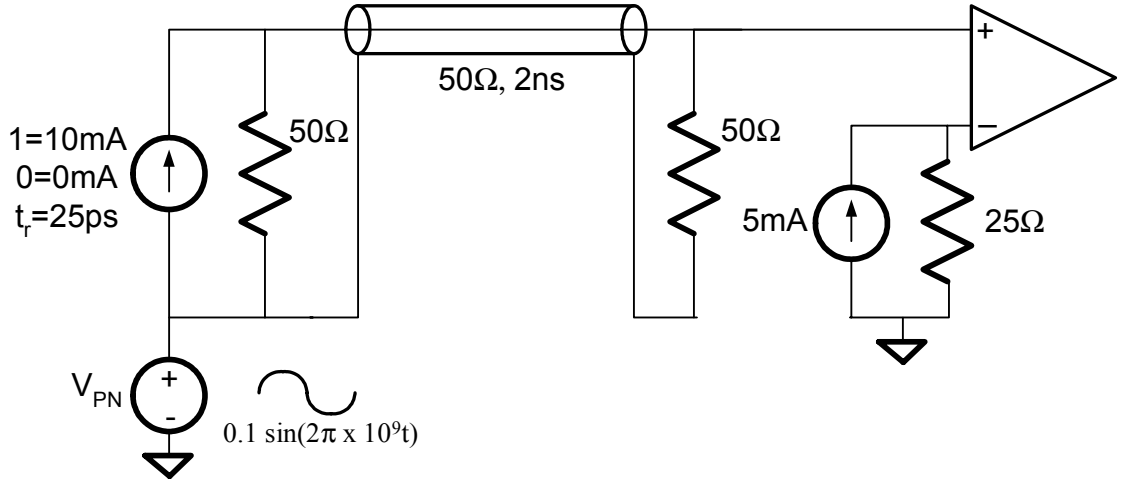
B. (5 points) Case 2:



$M = 1/2\ M_1$
$L = 1/2\ L_1$
$C_c = 2\ C_c$
$Cm = 2\ Cm_1$
$R = R_1$
$Z_0 = 1/2\ Z_0$
$Z_{even} = 1/2\ Z_{even}$
$Z_{odd} = 1/2\ Z_{odd}$
$V = V_1$

Problem 5: Advanced Signaling (20 Points Total)

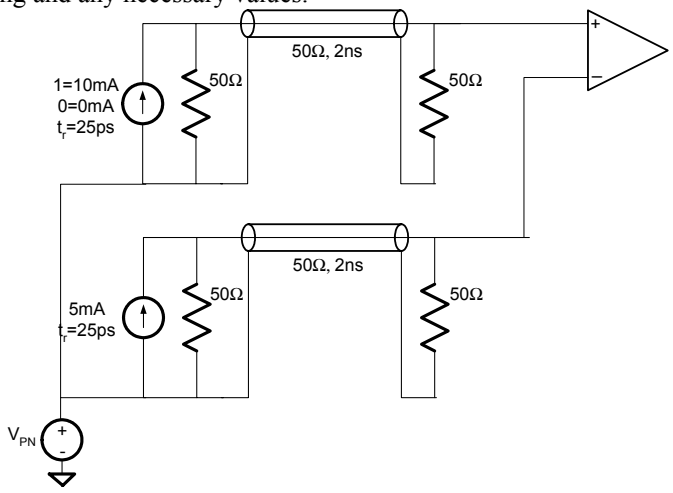
Consider the 2Gb/s signaling system shown below. The system is a single-ended unipolar signaling system that uses a 10mA driver with a 25ps rise time. Matched terminations of exactly 50 Ω are used at both ends of the line. The reference is generated by a 5mA driver across a 25 Ω resistor. Assume drivers and terminations are ideal. The power supply noise between the ground at the receiver and the ground at the transmitter is modeled by the voltage source V_{PN} in the diagram below. The power supply noise is modeled as a 100mV sin wave at a frequency of 1 GHz.



A. (5 points) What is the power supply noise that you must include in your noise budget?

Tx ground and Rx ground is different. The reference generator can not cancel out this noise. Power supply noise 0.1 V should be included

B. (5 points) Propose a method for reducing or cancelling the power supply noise, V_{PN}, by modifying the reference. Sketch a diagram of your system below. Be sure to include any assumptions you are making and any necessary values.



-3 point

To cancel out Vpn, reference should use same ground as transmitter. To make this scheme work, each transmission line should be the same(Z0 and Td should be the same). Terminal resistance should also be the same. -2 point

C. (5 points) Which of the following noise sources will be cancelled or reduced by your proposed system of part B? Crosstalk, receiver offset, signal return crosstalk, impedance mismatch, parameter mismatch, timing jitter. Give reasons to justify your answers.

Crosstalk, receiver offset, signal return crosstalk and impedance mismatch can not be reduced by the change of reference.

By generating reference near the transmitter, noise injected to nearby component with same amplitude can be cancelled out. Supply noise can be cancelled out by injecting same noise on the tx and reference, timing jitter can be also reduced since the reference has the same timing jitter as tx. Parameter mismatch can be also reduced since device on nearby location has much small variance than device located far away.

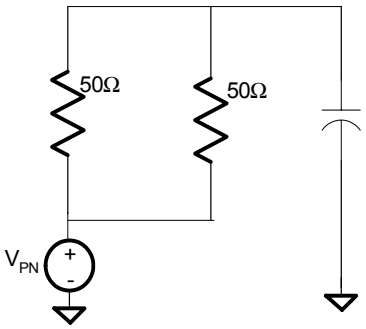
D. (5 points) To impress your boss, you decide to conserve money by using your modified reference of part B to act as the reference for 10 equivalent receivers. Each receiver has an input capacitance of 10pF at each input. How much power supply noise must you now include in your noise budget? Will the system still work?

If reference is made in each line, reference and the receiver have the same noise and supply noise can be completely cancelled out. But shared reference cause mismatch between those lines.

This problem can be solved with approximation or with exact solution.

i) Approximation

Assume input capacitance cause delay and phase change on the noise.



Reference Delay = RC = 25Ω*100pF = 2.5 ns

Rx node delay = 0.25ns,

Delay diffence is 2.25ns, this leads to phase difference in the noise

gnd noise is 0.1 sin(2π 1e9(t-2.25n)) – 0.1sin(2π 1e9 t) = 0.1*(2)^0.5*cos(2π 1e9 t+π/4)

amplitude of the noise is 0.141 V. This is more than gross margin of the system.

ii)

Since the transmission line is ideal, you have 0.1V supply noise on the receiver ground. Rx node has

$$\frac{1/j\omega C}{R+1/j\omega C}\cdot Vpn=\frac{1/j\cdot 2\pi 1e9\cdot 10e-12}{25+1/j\cdot 2\pi 1e9\cdot 10e-12}\cdot Vpn=0.537e^{j(-1.0)}\cdot Vpn$$

⇨ amplitude 0.0537 V, phase –1.0 =

On the reference, there are 10 capacitors. The noise is

$$\frac{1/j\omega C}{R+1/j\omega C}\cdot Vpn=\frac{1/j\cdot 2\pi 1e9\cdot 100e-12}{25+1/j\cdot 2\pi 1e9\cdot 100e-12}\cdot Vpn=0.06353e^{j(-1.51)}\cdot Vpn$$

The remaining noise is $(0.0537e^{j(-1.0)} - 0.06353e^{j(-1.51)})Vpn,= 0.482e^{j(-0.94)}$ Vpn

Therefore it has noise with amplitude 0.0482V . This is 40% of gross margin. This system is not working properly.