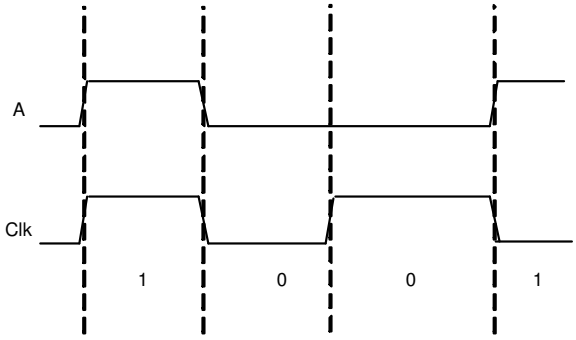
Homework 6 - Solutions

1 Problem 9-1 (Dally and Poulton)

Aperiodic Signal Encoding: Design a signal encoding that uses the minimum number of transitions and for which one of the signal lines always reflects the logical value of the signal.

There are many ways for the solution. If same number of transition can be achievable with those methods, those can be an answer, too.

Here's the one of the simplest answer for this problem. One line should represent the logical value of the line. To minimize the transitions, timing information should be in the other line to indicate a bit period. And both negative edge and positive edge should be used to minimize transitions. This is clocked NRZ encoding (see figure 9-17(c) in the book).

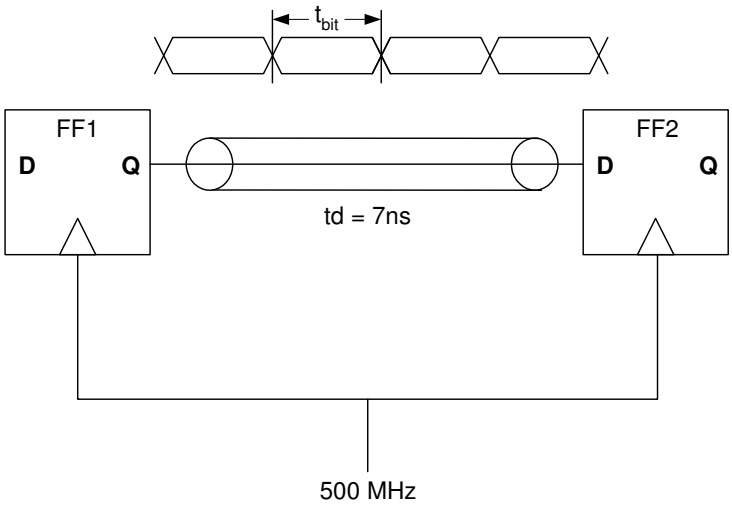


2 Problem 9-3 (Dally and Poulton)

Operating Range for Synchronous Timing: Consider a system that operates at 500Mb/s using synchronous timing, as shown in Figure 9-58. A communications link in this system includes a 7-ns (3 1/2-bit-long) transmission line. The link has a rise-time of $t_r = 1ns$, an aperture time, $t_a = 300ps$, and a timing uncertainty (skew + jitter) of $t_u = 300ps$. Over what ranges of clock frequencies will the link operate with correct timing?

The data travels on the link from FF1 to FF2. The delay of the wire is $t_{wire} = 7ns$.

If there were no timing uncertainty and no required aperture time and rise time, the maximum delay of the wire would be:



$$t_{wire} \leq 4t_{bit}$$

I.e. as long as FF2 were clocking at some time less than the transition of the fifth bit, the fourth bit would get clocked correctly through FF2.

However, we do have timing uncertainty in our system and a required aperture time and rise time. So, our maximum wire delay is actually:

$$\boxed{t_{wire} \leq 4t_{bit} - [0.5(t_r + t_a) + t_u]}$$

Manipulating this equation, we solve for t_{bit} and get:

$$t_{bit} \geq \frac{7ns + 0.5(1ns + 300ps) + 300ps}{4} = 1.99ns$$
$$ClockFrequency \leq 503MHz$$

For the worst-case minimum delay we perform a similar analysis.

Again, if there were no timing uncertainty and no required aperture time and rise time, the minimum delay of the wire would be:

$$t_{wire} \geq 3t_{bit}$$

I.e. as long as FF2 were clocking some time after the transition of the 4th bit, $\geq 3t_{bit}$, the fourth bit would get clocked correctly through FF2.

However, again, we do have timing uncertainty in our system and a designated aperture time and rise time. So, our minimum wire delay is actually:

$$\boxed{t_{wire} \geq 3t_{bit} + [0.5(t_r + t_a) + t_u]}$$

Manipulating this equation, we solve for t_{bit} and get:

$$t_{bit} \leq \frac{7ns - 0.5(1ns + 300ps) - 300ps}{3} = 2.02ns$$

$$ClockFrequency \geq 496MHz$$

Thus, the link works for the following clock frequency range:

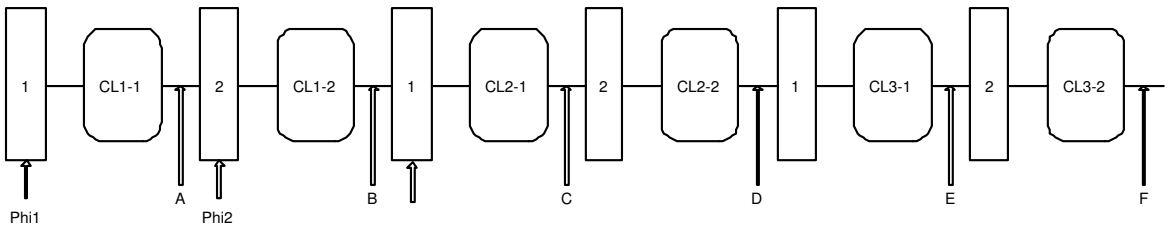
$$\boxed{496MHz \leq ClockFrequency \leq 503MHz}$$

At clock frequencies outside of this range, the above constraints will not be satisfied and the system will fail.

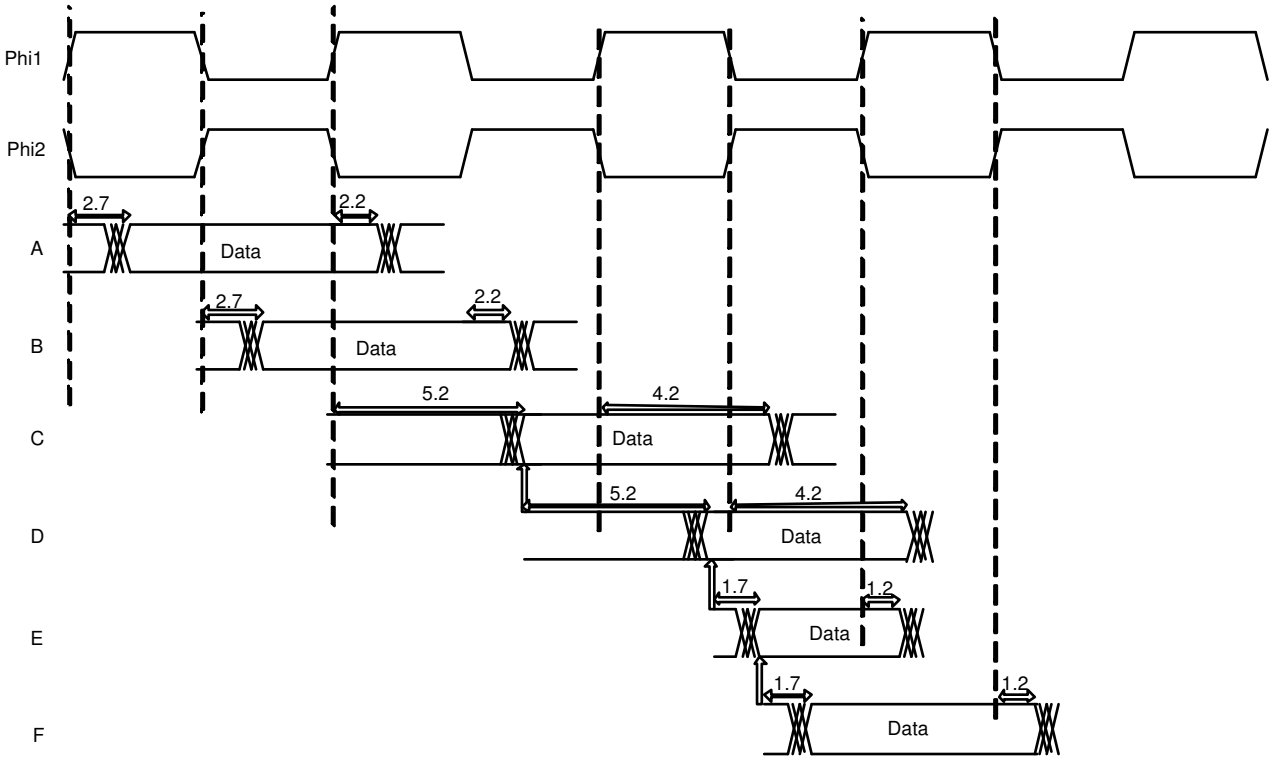
3 Problem 9-8 (Dally and Poulton)

Time Borrowing: Suppose the pipeline of Exercise 9-7 used level-sensitive latches rather than edge-triggered flip-flops with each stage broken down into two combinational logic blocks with half the propagation and contamination delays shown in Table 9-7. How fast can this pipeline operate using synchronous, level-sensitive timing? Make sure you account for borrowing time between pipeline stages. Assume the laches have a t_{dDQ} of 0.2 ns (half the flip-flop t_s + t_{dDQ}).

Each pipeline stage is split into 2 combinational logic, and latch with phi2 clock is inserted. Here's the figure for pipeline structure. CL represent combinational logic, and rectangle with '1' represent latch with phi1 clock.



Now let's work on the waveform that above structure generate. Since the bottle neck is on the 2nd stage(which has longest delay), we can find minimum cycle time constraint on that stage. Combinational logic has propagation delay from the positive edge of the clock or data from the previous stage. The slowest between those two will determine starting point of propagation delay. Contamination delay is from the positive edge of the clock for each stage. Each CL delay included 0.2ns of T_{dCQ} or T_{dDQ}. For example, propagation delay of the first stage is Half of CL + T_{dCQ} = $5ns/2$ + 0.2ns = 2.7ns



From above waveform, we can find some constraint on the cycle time. The falling edge of the clock should be later than the evaluation of the CL. On C, $5.2ns < T_{cycle}$. On D, $5.2ns + 5.2ns < 3/2 * T_{cycle}$. And on E $5.2ns + 5.2ns + 1.7ns < 2T_{cycle}$. Fastest T_{cycle} possible is 6.93ns.