Homework 5 - Solutions

1 Problem 5-4 (Dally and Poulton)

Series Regulator: Consider the circuit of Figure 5-28(b) where L=10nH and the load current, I_L, has the profile shown for I_1 in Figure 5-27. The clock period is 100ns. How large a bypass capacitor, C_B, is required to limit ripple on the 2.5-V supply at the load, V_L, to ± 5% if there is no series regulator? How large a bypass capacitor is required if a series regulator drops a 3.3-V distribution supply down to a 2.5-V load supply? What happens to the total power drawn from the supply in this case? (clock cycle is 50ns)

The value of the bypass capacitor without series regulation will be the same as in the first part of the previous problem. First calculate the Capacitance value:

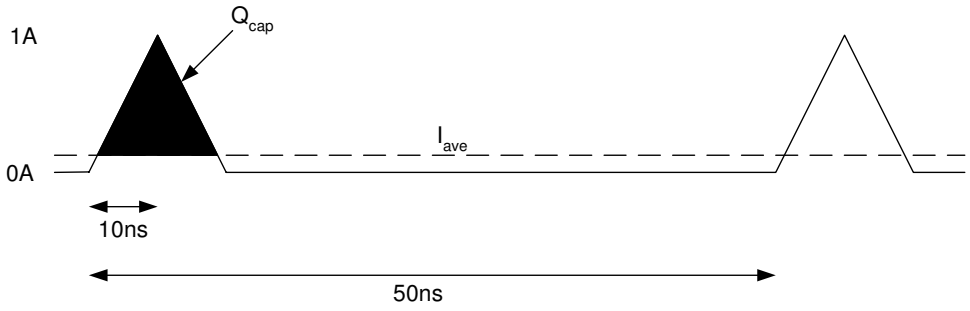
The current required by the load is shown below:

We begin by calculating the required Capacitance, C_B, for the bypass capacitor without shunt regulation. Our maximum voltage ripple is:

$$\Delta V = 0.05 \times 2.5V = 125mV$$

We calculate the average current as:

$$I_{ave} = \frac{Q_{Total}}{t_{ck}} = \frac{10ns * 1A}{50ns} = \boxed{200mA}$$



Now we calculate the charge that needs to be supplied by the bypass capacitor. This is the darkened area above I_{ave}, shown in the figure above:

$$Q_{cap} = 8ns \times 0.8A = 6.4nC$$

Solving for the bypass capacitor we have:

$$C_B > L\left(\frac{I_{ave}}{\Delta V}\right)^2 + \frac{Q_{cap}}{\Delta V} = 10nH\left(\frac{200mA}{125mV}\right)^2 + \frac{6.4nC}{125mV} = \boxed{76.8nF}$$

After adding the series regulator, the ΔV of the bypass capacitor increases to:

$$\Delta V = 3.3V - (2.5V \times 0.95) = \boxed{925mV}$$

The other values, I_{ave} and Q_{cap}, is calculated above.

$$C_B > 10nH\left(\frac{200mA}{925mV}\right)^2 + \frac{6.4nC}{925mV} = \boxed{7.39nF}$$

The power drawn from the supply with the series regulator is:

$$P_{supply} = I_{ave} \times V_{supply} = 200mA \times 3.3V = \boxed{660mW}$$

This is an increase of 33% in the power drawn from the supply.

2 Problem 5-12 (Dally and Poulton)

Bypass Capacitor Selection:

Using the parameters of Table 5-2, derive a parallel combination of bypass capacitors that is able to supply the current needs of a load with the periodic triangular waveform sketched in Figure 5-31 that may start and stop abruptly. Your combined capacitor should hold voltage ripple to within 5% of the supply voltage. Assume that your capacitors are fed from a DC supply voltage of 3.3V through an inductance of 1 μH.

We want to size our bypass capacitors so that the the maximum ΔV seen at the load is: $0.05 \times 3.3V = \boxed{165mV}$.

A solution is shown below. There are a myriad of possibilities. For all possibilities, the methods used below should be used.

First rank:

We size our first rank capacitors based on 3 criteria:

1. The ΔV of this capacitor when it is supplying the AC current should be kept less than 165mV.
2. The inductance of this bypass capacitor should be such that the voltage across the series inductance will be less than 165mV. (Technically, the sum of 1 and 2 should be kept less than 165mV. Since the series inductance of the on-chip capacitors is 0, this criteria ends up not being an issue.)
3. The capacitor must be acting as a capacitor for the highest frequency seen at the load: $\frac{1}{t_{rise}} = 1GHz$. I.e. we want the frequency breakpoints to be above our highest frequency.

First we find the average current and the charge that is sourced by the bypass capacitor:

$$I_{ave} = \frac{10A \times 1ns}{6ns} = \boxed{1.67A}$$

$$Q_{cap} = (1ns - 0.167ns)(10 - 1.67A) = \boxed{6.94nC}$$

From the first criterion above, we have:

$$C_{rank1} > \frac{Q_{cap}}{\Delta V} = \frac{6.94nC}{165mV} = \boxed{42nF}$$

From the second criterion we have:

$$L_{rank1} < \frac{\Delta V}{\frac{di}{dt}} = \frac{165mV}{\frac{10A}{1ns}} = 16.5pH$$

From the third criterion, we must have a capacitor that's breakpoint frequencies are above 1 GHz ($\frac{1}{t_rise}$).

From Table 5-2, we notice that the only capacitors that will allow for the third criterion are the on-chip MOS capacitors. We choose the second option (line 2 of the Table 5-2) since these capacitors are more area efficient. We also notice that these capacitors have no series inductance, so the second criterion above is met. Thus, all of the above criteria are met.

The minimum number of SMT MOS capacitors we'd need to choose is 42,000 1pF on-chip MOS capacitors. We choose a value of 60,000 1pF on-chip MOS capacitors.

So our first rank of capacitors has the specification:

$$C_{rank1} = 60nF, L_{rank1} = 0, R_{rank1} = \frac{40\Omega}{60000} = 6.67 \times 10^{-4}\Omega$$

This resistance value is negligible.

Second rank:

Now we specify the previous rank, second rank, in bypass capacitor network. We use the specification:

$$L_{rank+1} < C_{rank}\left(\frac{\Delta V}{I_{ave}}\right)^2$$

Thus, we have:

$$L_{rank2} < 60nF\left(\frac{165mV}{1.67A}\right)^2 = 586pH$$

We note that we cannot directly hook up the first rank up to the supply voltage since the supply inductance, 1 μH, does not satisfy the above criterion.

We choose to use 12 SMT ceramic capacitors (line 4 of Table 5-2) to satisfy the above criterion. Choosing this value satisfies the inductance calculation above as well as doubling the capacitance of the first rank.

Our second rank of capacitors has the specification:

$$C_{rank2} = 120nF, L_{rank2} = \frac{1nH}{12} = 83.3pH, R_{rank2} = \frac{0.1\Omega}{12} = 0.00833\Omega$$

Third rank:

$$L_{rank3} < 120nF\left(\frac{165mV}{1.67A}\right)^2 = 1.17nH$$

,which is just double our previous value. Since this value is not greater than or equal to the voltage source inductance, we need to add the third rank of capacitors.

We use 11 aluminum electrolytic capacitors (sixth line of table 5-2).

Our third rank of capacitors has the specification:

$$C_{rank3} = 110\mu F, L_{rank3} = \frac{10nH}{11} = 909pH, R_{rank3} = \frac{1\Omega}{11} = 0.091\Omega$$

We note that this is a significant resistance value and the maximum voltage dropped across this resistor is: $0.091\Omega \times 10A = 910mV$. This is not an acceptable value since our maximum voltage ripple is 165mV. So, we need to reduce our resistance to: $R_{rank3} = \frac{165mV}{10A} = 0.0165\Omega$. Note: this is a conservative estimate. Thus we choose to use 60 Aluminum electrolytic capacitors. Our new values are:

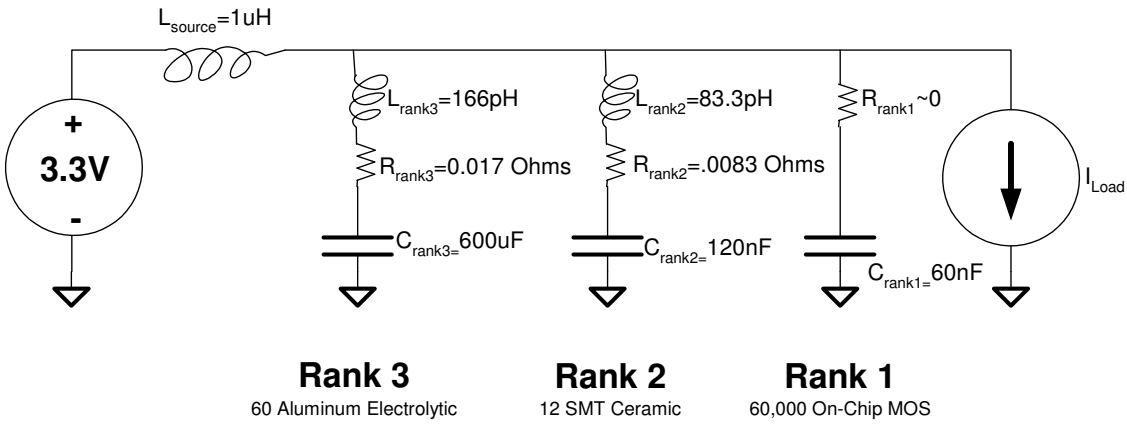
$$C_{rank3} = 600\mu F, L_{rank3} = \frac{10nH}{60} = 166pH, R_{rank1} = \frac{1\Omega}{60} = 0.0167\Omega$$

We now design for our fourth rank of bypass capacitors:

$$L_{rank4} < 600\mu F\left(\frac{165mV}{1.67A}\right)^2 = 5.86\mu H$$

The inductance of the supply voltage, 1μH, satisfies this criterion, so we don't need to add a fourth rank of bypass capacitors and we're done.

The designed bypass capacitor network is shown in the figure below.



We Spice our circuit to verify that our design keeps the voltage ripple on the load within ± 165mV.

We use the following Spice netlist:

```
* Problem 5-12 .option post

.param vdd = 3.3V

* DC source
   V0 a0 gnd vdd
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```
    l0 a0 a 1uH

* Rank 1
    r0 a b 0.00067
    c0 b gnd 60nF

* Rank 2
    l1 a c 83.333pH
    r1 c d 0.0083
    c1 d gnd 120nF

* Rank 3
    l2 a e 166pH
    r2 e f 0.0165
    c2 f gnd 600uF

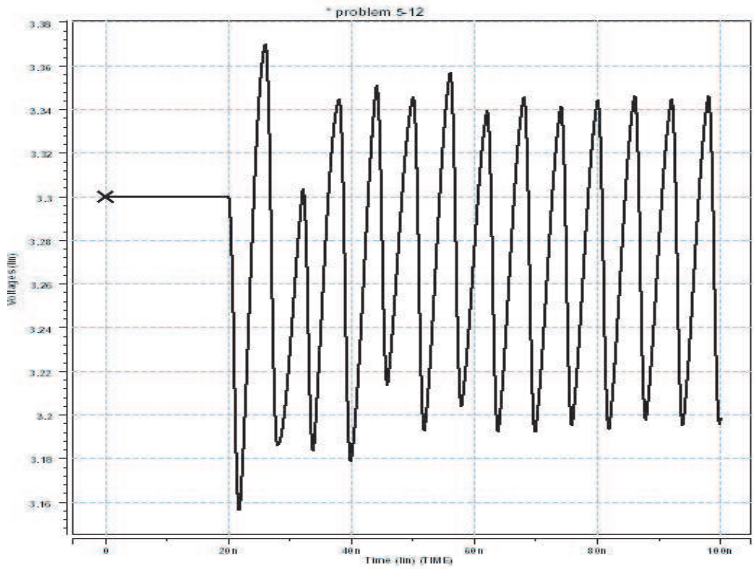
* Current Load
    I1 a gnd pulse 0 10 20n 1n 1n 0 6n

* Note that we delay the above current load by 20ns to simulate the current starting/stopping abruptly.

.tran 1ps 100ns

.end
```

We obtain the following voltage waveform at the load:



We note that the maximum voltage variation on the output does not exceed ± 165mV (i.e. the ripple doesn't exceed 3.465mV and it doesn't go lower than 3.14mV). We have met our design specifications.

It's important to note that in practice after getting an initial solution to the distribution problem, an engineer iterates trying alternative solutions to find the lowest-cost solution with acceptable performance.

3 Problem 5-13 (Dally and Poulton)

IR Drops : Design a power distribution network for a peripherally bonded ASIC. Your chip is 15 × 15 mm in area and contains 1M gate equivalents. Each gate equivalent drives a 200-fF load (40fF of gate and 160fF of wire) and switches on average every third cycle of a 100MHz clock. What is the total power dissipation of your chip? Assuming a peak current to average current ratio of 4:1, what fraction of a metal layer(or how many metal layers) do you need to distribute power so the overall supply fluctuation of a 2.5V supply is ± 250 mV?

$$I_{avg} = C\frac{dV}{dt} = \frac{1}{3} * 1M * 200fF * 2.5V * 100MHz = 16.67A$$

$$J_{avg} = I_{avg}/(15mm)^2 \ = 0.0740A/mm^2$$

$$J_{peak} = 4J_{avg} = 0.296A/mm^2$$

Therefore, the number of metal layer is

$$K_p = \frac{r_W \cdot L^2 \cdot J_{peak}}{8 \cdot V} = \frac{0.04 \cdot (15)^2 \cdot 0.296}{8 \cdot 0.25} = 1.332$$

If you think that actual supply fluctuation is between the gnd and vdd, each layer has less than ± 125 mV fuctuation. Therefore, for each of gnd and vdd,

$$K_p = \frac{r_W \cdot L^2 \cdot J_{peak}}{8 \cdot V} = \frac{0.04 \cdot (15)^2 \cdot 0.296}{8 \cdot 0.125} = 2.664$$

both of those answers have full credit.