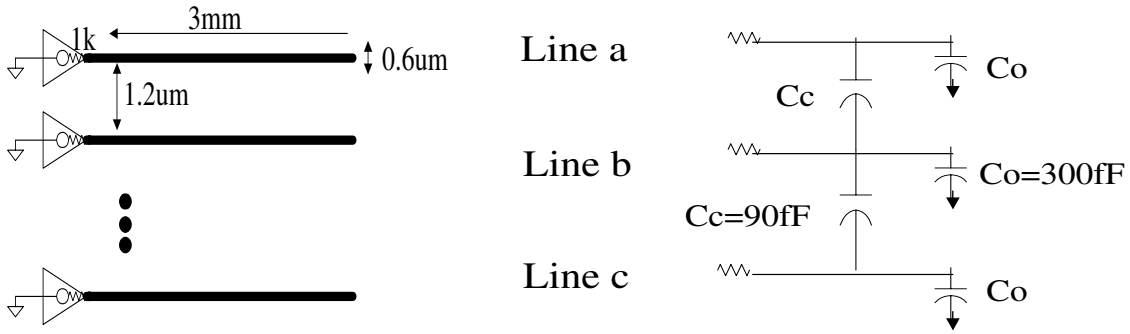
Homework 3 - Solutions

1 Problem 6-3 (Dally and Poulton)

Capacitive Cross Talk and Delay : You are designing a chip that has a 3-mm-long data bus of 0.6um wires on 1.2 um centers. Assume the capacitance numbers from Table 6-2 and asssume that the perpendicular wires on adjavent layers are all grounded. You are driving each bus line with a static driver that can accurately be modeled as a voltage source in series with a 1 kΩ resistor. Assume that all lines switch simultaneously to random states, what is the worst-case maximum and minimum delay of a line(give an RC time constant)? (Hint: What combination of transitions on adjacent lines will speed up or slow down a transition on a given bit?)

For the problem, you can approximate that the resistance of the wires will be much smaller than 1kΩ of driver. For example, in 0.35um process, Rsq = 0.02 for top level metal probably to be used for global interconnect. In this case Rwire = 99Ω, which is much smaller than 1kΩ. So, ignore the resistance of the wire for this problem



(a) circuit (b) modeling

Figure 1: Problem 6-3

Using table 6-2.

$$Co = C(top) + C(bottom) = 2 * (C(parallel) + C(fringe))$$

$$= 2 * (3mm * (0.6um * 0.05fF/um^2 + 2 * 0.01fF/um)) = 300fF$$

Note that for the fringe effect, there are left and right sides in the wire. Therefore, it should be 2*0.01fF/um.

$$Cc = C(side) = 0.03fF/um * 3mm = 90fF$$

What is the worst case condition of transitions which will cause the maximum delay? That is the case when the effective capacitance is maximum value. If the two side aggressor lines transitions in the opposite direction of the main driver on the victim line, this will create the most amount of capacitance due to the Miller effect. Victim line will see approximately twice the capacitance from both of the aggressor lines.

$$C(total) = Cs + 2 * Cc + 2 * Cc = 300fF + 2 * 90fF + 2 * 90fF = 660fF$$

For resistance = 1kΩ

$$R * C = 660ps$$

The fastest delay is when the aggressor lines switch to the same direction, so there is no coupling capacitance.

$$C(total) = Cs = 300fF$$

$$R * C = 300ps$$

2 Problem 6-5 (Dally and Poulton)

Transmission-Line Cross Talk : Your printed-circuit layout contractor has inadvertently run a full-swing(3.3V) CMOS signal with a fast 500ps rise time right next to a low-swing(300mv) signal for a 10cm run of microstrip line. The lines are each 8mils wide spaced 6 mils above a ground plane and spaced 8 mils from one another, a geometry that matches the first line of Table 6-3. Both lines are parallel terminated at the receiving end only. What is the magnitude of the noise induced on the low-swing line? Is that a concern?

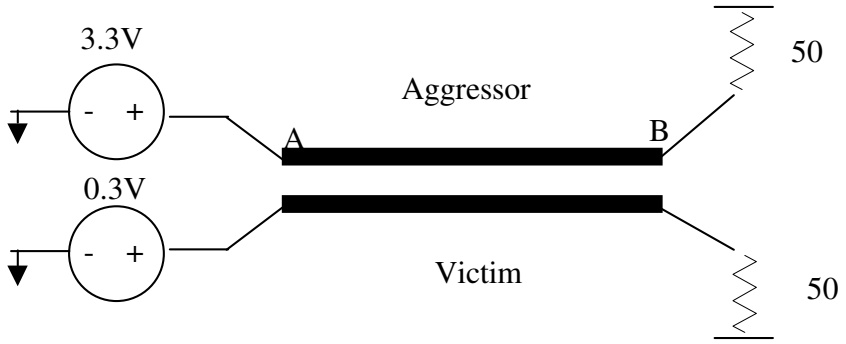


Figure 2: Problem 6-5

From table 6-3. We can get

$$k_{fx} = -0.047, \quad k_{rx} = 0.058$$

The voltage step(Since the rise time is very short, we can assume this) on the aggressor line makes crosstalk on the victim line at the farend. The velocity of the waves can be calculated from L and C values on the tables. Since victim line has small swing compared to the aggressor line you can ignore Miller effect. C=C+Cm = 88+6.4 = 94.4 pF/m, L = 355 nH/m, so v = $\frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{94.4pF/m * 355nH/m}} = 1.73 \times 10^8$ m/s. Therefore t_x = 10 cm / $1.73 \times 10^8 = 0.578$ ns. In the worst case, farend crosstalk and nearend crosstalk will be added. So add absolute value of each of these.

Crosstalk from the aggressor to Victim is:

$$V_{xtalk} = k_{fx} * t_x * \frac{\Delta V_{aggressor}}{\Delta t} + \Delta V_{aggressor} * k_{rx} * k_r$$

$$= 0.047 * 0.578ns * 3.3/500ps + 3.3 * 0.058 * 1 = 0.37$$

One thing to be careful is that victim line also makes crosstalk on the aggressor and this makes another crosstalk on the victim line. There are also 3rd, 4th effect on this, but those can be ignored. Just consider 2ndary effect only.

Therefore total noise from the crosstalk is 0.37 V. This is bigger than noise margin = 300mV/2 = 150mV. This will cause problem to this system.

3 Problem 6-7 (Dally and Poulton)

Signal-Return Cross Talk : Your have an integrated circuit package that can be accurately modelled as a lumped 5nH inductor for each pin. You plan to use this package to house a chip that drives 128 full-swing(3.3 V) outputs into 50 Ω lines with 1ns rise times. How many return pins do you need if the drop across the return s must be kept less than 300mV in the worst case? How many returns are needed if the rise time is slowed to 3ns?

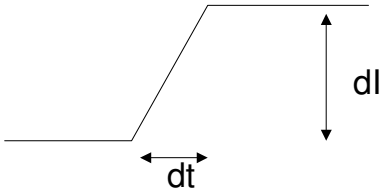


Figure 3: Problem 6-7

We can assume the current ramp up in in the same rise time as the voltage swing. For the worst case, all the full voltage swing goes to the same direction and maximum current will be drawn through pin. Then total current change will be

$$\Delta I = \frac{\Delta V}{R} * 128 = \frac{3.3}{50} * 128 = 8.448A$$

Then inductance should be less than

$$L\frac{\Delta I}{\Delta t} \leq V = 300mV$$
$$L \leq 0.355nH$$

To reduce inductance use parallel connection of inductance by using multiple pins.(n = number of pins)

$$\frac{L}{n} \leq 0.355nH, \quad n \geq 140.8$$

at least 141 pins are needed.

When rise time = 3ns, similarly

$$n \geq \frac{L}{V}\frac{\Delta I}{\Delta t}, \quad n \geq 46.9$$

at least 47 pins are needed.

4 Problem 6-15 (Dally and Poulton)

Statistical Analysis of Bounded Sources: Consider a system with $\Delta V = 250$mV. Fixed-noise sources have a magnitude of $V_{NI} = 50$mV. Correlated-noise sources(datapath bits that may all switch simultaneously) are modelled by $K_N = 0.20$. In addition, the signal crosses 100 perpendicular signals whose transitions are uncorrelated. The worst-case noise due to capacitive cross talk from each of these perpendicular signal is $K_N = 0.005$(or 1.25 mV). If you perform a worst-case analysis, will the system work? If you model the 100 perpendicular signals as a statistical source, what is its rms voltage level? What is the predicted BER using the statistical model?

(i) using worst case analysis on the perpendicular signals

Gross Margin : $\frac{250}{2} = 125$ mV

Fixed noise : $N_i = 50$ mV

Correlated noise : $K_N = K_N(datapath) + K_N(perpendicular) = 0.2 + 100 * 0.005 = 0.7$

Bounded Noise : 50mV + 0.7*250 mV = 225 mV

Net Margin : -100mV

Net margin is negative, therefore this system can not work according to this noise analysis.

(ii) using statistical model on the perpendicular signals

Let's calculate rms voltage level for the 100 perpendicular line

First, let's calculate an rms noise voltage from one vertical line. We can assume that rise and fall on the signal happen with same probability.

$$V_1 = \begin{cases} +K_n * \Delta V & \text{with probability } \frac{1}{2} \\ -K_n * \Delta V & \text{with probability } \frac{1}{2} \end{cases}$$

$$E(V_1) = (+K_n * \Delta V)\frac{1}{2} + (-K_n * \Delta V)\frac{1}{2} = 0$$

$$\sigma(\text{rms value}) = \sqrt{var(V_1)} = \sqrt{E(V_1^2) - (E(V_1))^2} = \sqrt{E(V_1^2) - 0}$$

$$= \sqrt{(+K_n * \Delta V)^2\frac{1}{2} + (-K_n * \Delta V)^2\frac{1}{2}} = K_n * \Delta V$$

Now, consider the noise comes from 100 independent lines

$$V_r = V_1 + V_2 ... V_{100}$$

$$V_{r(rms)} = \sqrt{V_{1(rms)}^2 + V_{2(rms)}^2 ... V_{100(rms)}^2} = \sqrt{100 * V_{1(rms)}^2}$$

$$\rightarrow V_{r(rms)} = 10V_{1(rms)}$$

Therefore rms voltage level is

$$V_{r(rms)} = 10(K_n * \Delta V) = 12.5mV$$

Assume that there are no other statistical noise source except for the noise from perpendicular lines.

Gross Margin : $\frac{250}{2} = 125$ mV

Fixed noise : $N_i = 50$ mV

Correlated noise : $K_N = K_N(datapath) = 0.2$

Bounded Noise : 50mV + 0.2*250 mV = 100 mV
Net Margin : 25mV

Standard deviation of the noise(rms voltage level) $V_R = \sigma(K_N * 250mV) = 12.5$ mV

VSNR : $\frac{V_M}{V_R} = 2$

BER : exp(-$\frac{VSNR^2}{2}$) = 0.135