EE273 Digital Systems Engineering Final Exam

March 19, 2003

(Total time = 120 minutes, Total Points = 100)

Name: (please print)_____

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature:_____

This examination is open notes open book. You may not, however, collaborate in any manner on this exam. You have two hours to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary.

Before starting, please check to make sure that you have all 10 pages.

1		**52**
2		**20**
3		**10**
4		**18**
Total		**100**

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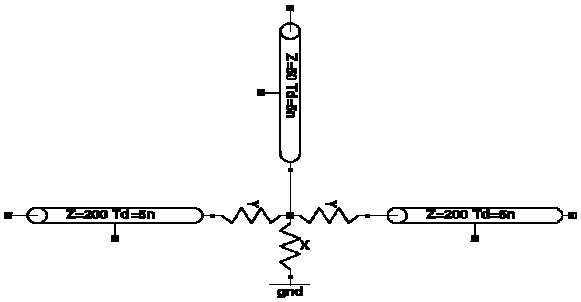
Problem 1: Short Answer (52 Points: 13 questions, 4 points each)

A. Sketch a resistor network that can be placed between a 50-Ohm transmission line, and two 200-Ohm transmission lines so that waves propagating in any one of the 3 lines passing toward the network will be passed on to the other two lines with no reflections.



50 = X || (Y+200)/2

200 = Y + X||50||(Y+75)

from above equations

X = 68 Ω Y = 176.5Ω

B. Suppose you have a canonical brute-force synchronizer with a waiting time of t_w = 1.8ns, t_{cy} = 2ns and a failure probability of $P_F = 10^{-30}$. The aperture time, t_a, is 50ps. If the regeneration time constant, τ_s, is doubled with no other changes, what will the new failure probability be?

$$P_{F-old} = \frac{t_a}{t_{cy}} \exp(-\frac{t_w}{t_s}) = 10^{-30} = \frac{0.05ns}{2ns} \exp(-\frac{t_w}{t_s})$$

$$P_{F-new} = \frac{t_a}{t_{cy}} \exp(-\frac{t_w}{2t_s}) = P_{F-old} \exp(\frac{t_w}{2t_s}) = 1.58 \cdot 10^{-16}$$

C. You are using a current-mode bipolar differential signaling system. In the current system the net margin is 50mV, the gross margin is 400mV and the proportional noise constant, k_n, is 0.4. The bit error rate of the current system is 10^{-5}. You find that this bit error rate is not acceptable and decide to double the current drive. How does this improve the BER? Give a number.

BER= exp(-1/2(50mV/Vn)$^{-2}$) = 10^{-5} , => Vn = 10.42mV*
*Vnoise = 0.4*Vswing + Vfixed = Vgm-Vnm = 350mV => Vfixed = 30mV*
*Vgm(new) = 800mV, Vnoise(new) = 0.4*1600mV + 30mV = 670mV*
BET(new) = exp(-1/2((Vgm-Vnoise)/Vn)$^{-2}$) = 1.588*10^{-34}*

D. You are using the Motorola 100LVE111 to design a 3-stage clock tree. Each chip takes 1 clock input and fans it out to 9 outputs. The maximum skew between outputs on the same chip is 50ps. The maximum skew between outputs on two different chips with the same input is 200ps. Assuming no other timing uncertainty is introduced, what is the worst-case skew between two outputs at the leaves of the tree?

Worst case skew = First rank skew + Second + Third
= 50ps + 200ps + 200ps
=450ps

E. A chip is operating at 2.5V, draws a peak current of 30A and an average current of 10A. The bypass network must handle the transient when the chip switches to standby mode, and the average current switches from 10A to 0A, with a maximum change in voltage of ±10%. The cycle time is 1ns. What is the minimum value of the first rank of on-chip bypass capacitors that will satisfy this constraint?

Iavg = 10A

$$C_B > (\frac{I_{avg}}{\Delta V_{\max}})^2 L + \frac{k_i I_{avg}}{\Delta V_{\max}} t_{ck} = (\frac{10}{0.25})^2 L + \frac{10}{0.25} 1ns$$

$$= 1600L + 40nF$$

F. A signaling system has a rise/fall time of 50ps, an aperture time of 75ps, jitter of ±80ps (160ps peak-to-peak), and operates using ***synchronous timing*** over a line with 2ns of delay. (a) What is the fastest rate at which this system can operate? (b) At the signaling rate found in part (a), how much peak-to-peak jitter in the oscillator (in addition to the ±80ps specified above) can this system tolerate before it stops functioning?

There are two possible solutions for this problem

i) $2n > (n-1)\, t_{cy} + (t_r + t_a)/2 + t_j$

$2n < n\, t_{cy} - ((t_r + t_a)/2 + t_j)$

$2.1425 / n < t_{cy} < 1.8575 /(n-1)$ n=7

$t_{cy} = 0.306ns$, data rate = 3.26 Gbps, no extra jitter allowed

ii) Bit period = 2ns/6.5bit = 307.7 ps , 3.25Gbps

Minimum bit time needed = 50ps + 75ps+ 160ps = 285ps

Extra jitter allowed = 307.7ps – 285ps = 22.7 ps

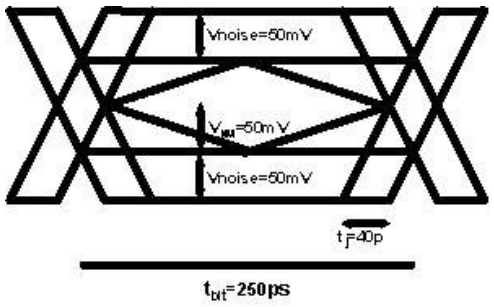
G. You have a signaling system with the same parameters as described in part F. I.e. t_r=50ps, t_a=75ps, t_j=±80ps. Again you are transmitting over a line with 2ns of delay. You decide to use ***pipeline timing***. What is the maximum rate at which this system can operate? How much peak-to-peak jitter in the oscillator (in addition to the ±80ps specified above) can this system tolerate before it stops functioning?

160ps peak to peak jitter

1/(50ps + 75ps + 160ps) = 3.5Gbps

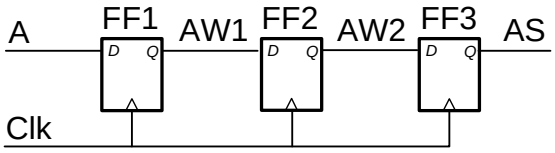
No extra jitter is allowed

H. A signaling system using per-line closed-loop timing has a bit time of 250ps, a rise/fall time of 50ps, ±40ps (80ps peak-to-peak) of bounded jitter plus Gaussian jitter with an RMS (1σ) value of 10ps. The signal swing is 200mV, the bounded noise sources total 50mV, and there is 5mV RMS Gaussian noise. What is the BER of this system due to the combination of voltage noise and timing noise?



Vswing = 200mV
Vn = 50mV
Vnm = 100mV – 50mV = 50mV
Vrms = 5mV
Vrms(from timing) =
*10ps * 100mV/(250ps-80ps)=5.88mV*
Vrms(total) = $(5.88^2+5^2)^{0.5}$ = 7.72mV
BER = exp(-1/2(50/7.72)^2) = 7.8e-10*

I. You are using the brute-force synchronizer shown below. Each flip-flop has a set-up time, t_s, of 50ps, a hold time, t_h, of 50ps, a data clock-to-Q time, t_{dCQ}, of 75ps and a regeneration time constant, τ_s, of 200ps. The clock is running at 2GHz. What is the probability of failure of this system? You are using this synchronizer to synchronize the inputs from a keyboard where the person types on average 300 keystrokes per minute. What is the frequency of failure of this system?



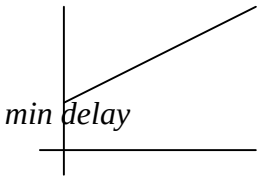
$$F_F = f\frac{t_a}{t_{cy}}\exp(-\frac{t_w}{t_s}) = 300/\min\cdot\frac{0.1ns}{0.5ns}\exp(-\frac{500\,ps*2-(75\,ps+50\,ps)*2}{200\,ps})$$

$$=1.411/\min$$

J. A plesiochronous three-register FIFO synchronizer moves a signal between two clock domains where the maximum frequency difference is 100ppm. Ignoring flip-flop non-idealities, what is the minimum rate at which NULLS must be put on the line to guarantee that data will not be duplicated or dropped? With this rate of added NULLS, what is the rate at which the rp pointer must be updated?

To compensate frequency difference, 100ppm NULL signal should be insere
*rp updated with NULL signal with rate of data rate*10^{-4}*

K. When using digital delay lines, why is a delay line with a smaller minimal insertion delay (such as a trombone delay line) preferred above a delay line (such as a multiplexer delay line) that has a large minimal insertion delay?

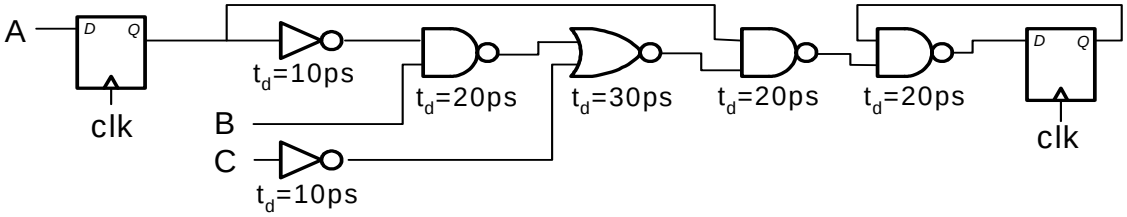


To reduce the jitter in the line since jitter is proportional to overall delay.

L. Suppose you want to use a two-register synchronizer to synchronize a mesochronous system running at 4 GHz. The flip-flops have a set-up time, t_s, of 75ps a hold time, t_h of 75ps, a clock-to-Q, t_{dCQ}, of 60ps and a contamination delay, t_{cCQ}, of 10ps. Will the two-register synchronizer work? If not, describe a method that will be guaranteed to work for this system. Sketch your solution.

Total timing uncertainty need to synch. t_s, + t_h + t_{dCQ} - t_{cCQ}, = 200ps > Tcy/2
This system will not work.
FIFO synchronizer can be used to increase valid time region.

M. In the figure below A, B and C are primary inputs and you may assume they are available at t=0. The two flip-flops are driven by the same clock source. However, due to varying path lengths, there is possible skew between the clock inputs to the two flipflops. The parameters of the two flip-flops are: t_{dCQ} = 10ps, t_s = 10ps, t_h = 20ps. Each gate has the delay listed in the figure. Find the maximum skew that the system can tolerate. With that maximum skew present, what is the maximum clock frequency at which this system can operate?

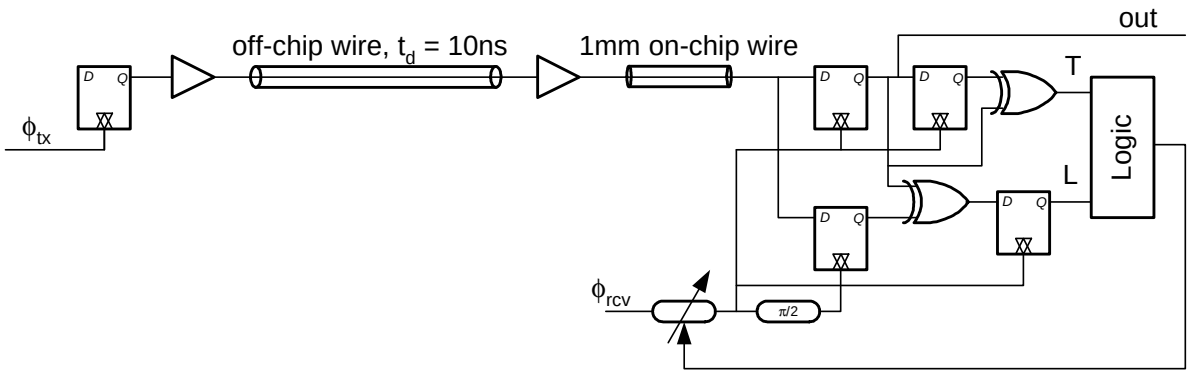


From the path through ff-NAND NAND –ff
Tcq + Tdmin > Tskew + Thold => 50 ps > Tskew + 20ps,
T skew < 30ps

The minmum cycle time is
Tcq + Tdmax + Tsetup + Tskew
= 10ps + 10ps + 20ps +30ps + 20ps + 20ps + 10ps + 30ps

= 150ps
fmax = 6.67 GHz

Problem 2: Timing Analysis [20 Points total]



Consider the transmission system shown above. A data signal is transmitted on each edge of a transmit clock. The specifications of the flip-flops, delay line, buffers, xor gates, and oscillators are shown in the table below. The rise/fall time of the signal is 25ps. ϕ_{tx} and ϕ_{rcv} are outputs of 2 separate oscillators. You may assume that ϕ_{tx} and ϕ_{rcv} have the exact same frequency but possibly different phases.

Component	Specification	Value	Units
Oscillator	Jitter	10	ps (p-p)
Flip-flop	Jitter	10	ps (p-p)
	Skew	±10	ps
	Aperture time	20	ps
	Aperture offset	±10	ps
Buffer	Jitter	15	ps (p-p)
	Skew	±20	ps
Delay line	Skew	10% of delay	
Xor gate	Jitter	5	ps (p-p)
	Skew	±5	ps

(a) [8 points] What is the fastest data rate at which this system will operate reliably?

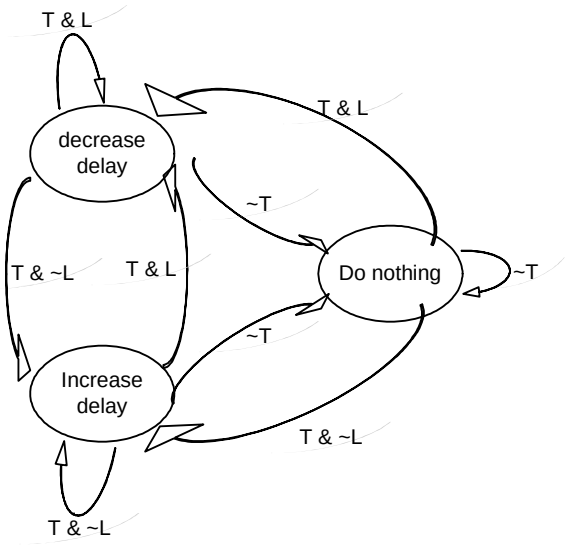
t_{jitter} = 10ps(oscillator)*2 + 15ps(Buffer)*2
$t_{skew(uncancelled)}$ = 20ps (phase comparator) + 1/2*U.I*0.1(delay line, in the worst case)

t_a = 20ps
t_r = 25ps
$t_{aperture,offset}$ = 20ps

t_u = 80ps + 0.05U.I.
U.I = t_a +t_r + $t_{aperture,offset}$ + t_u
U.I = 153ps

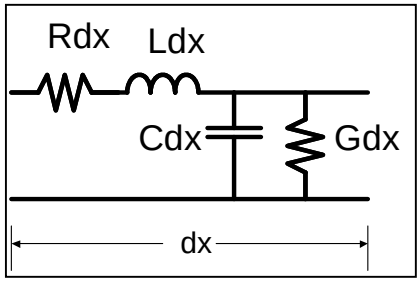
data rate = 6.55 Gbps

(b) [7 points] Draw the state diagram of the state machine inside the logic box above.



Note :
The output of the state machine (increase or decrease delay) should be low pass filtered

(c) [5 points] The line described in part (a) is surrounded by two identical lines, one above and one below. The buffers can be modeled as drivers with 1kOhm resistance. The 1mm on-chip wire has the infinitesimal wire model shown below with the following parameters: R=7Ω/m, L=300pH/m, C=200pF/m, G=0. 50pF/m of this capacitance is to the line above and 50pF/m is to the line below. The remaining 100pF/m of capacitance is to ground. You may assume the coupling between the off-chip portions of the line is 0. Does this change the fastest data rate of this system? If so, what is the fastest data rate at which this system will operate reliably?

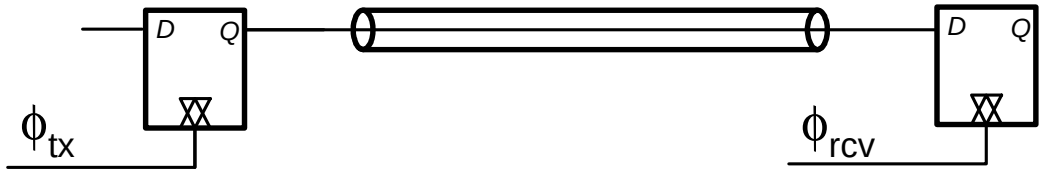


t_{jitter} (from Miller effect)
= R(C(aggressors changes to opposite dir) – C(aggressor changed to same dir)
= R((50pF+50pF)*2 +100pF– ((50pF+50pF)*0+100pF)) =*
(1k + 7Ω) 200pF = 201 ps

data rate = 1/(153ps + 201ps) = 2.8 Gbps

Problem 3: Periodic Synchronization [10 Points]

Suppose you are transmitting data at a different rate than the rate at which you are receiving data as shown below. The transmission rate, ϕ_{tx}, is 100 MHz and the receiving rate, $\phi_{rcv,}$ is 150 MHz.



(a) [8 points] Will the system operate correctly as drawn? If not, propose a method for fixing this system. Label all required signals and specify any timing or data constraints.

No, the system will not work .
We need to use a periodic synchronizer using a clock predictor as given in text.
Partial credit was also given for brute force synchronizers.

(c) [2 points] What is the added delay to the data path due to synchronization?

Tdcq – Tccq + Ts + Th + Tmux

Problem 4: Clock Trees and Synchronization [18 points total]

You are using a Motorola 100LVE111 to build a 2-level clock tree without any trimming on the outputs. The input oscillator is running at 2GHz.

(a) [4 points] Design a delay-line synchronizer that will synchronize a signal sent from one leaf of the tree to another leaf of the tree. Your synchronizer should add minimal delay to your system. Below is a list of parts with their respective parameters. If you use any additional parts, specify the appropriate parameters in your design.

Flip Flop	t_s = 20ps, t_h = 20ps, t_{dCQ} = 60ps, t_{cCQ}=10ps
Basic Gates (and, or, nor, nand, xor, etc.)	delay = 50ps
N-Input Mux	delay = 200ps

You could use any mesochronous synchronizer (delay line or two register or FIFO)

(b) [2 points] What is the added delay to your data path because of synchronization?

Delay = Tdcq – Tccq + Ts + Th + Tmux + 250ps = 340ps

(c) [9 points] You find that you have 800ps of p-p jitter in your system, and the above delay-line synchronizer will no longer work. Propose a synchronization method using a FIFO synchronizer that will work while adding a minimal amount of delay to your data. Sketch your system below. You may use the same parts listed in part (a). If you use any additional parts, specify the appropriate parameters in your design.

A two register FIFO synchronizer is sufficient.

(d) [3 points] What is the added delay to your data path because of synchronization in your design above? What is the change in data throughput between your synchronization system of part (c) and the synchronization system of part (a)?

Delay = 1 clock cycle + Tdcq + Tmux = 760ps