EE273 Digital Systems Engineering
Final Exam

March 16, 2000
(version 0.6ϕ)

(Total time = 120 minutes, Total Points = 100)

Name: (please print)_____

In recognition of and in the spirit of the Stanford University Honor Code, I certify that I will neither give nor receive unpermitted aid on this exam.

Signature:_____

This examination is open notes open book. You may not, however, collaborate in any manner on this exam. You have two hours to complete the exam. Please do all of your work on the exam itself. Attach any additional pages as necessary.

Before starting, please check to make sure that you have all 10 pages.

1		**20**
2		**15**
3		**16**
4		**24**
5		**25**
Total		**100**

Problem 1: Short Answer (20 Points: 10 questions, 2 points each)

A. Suppose you have a signaling system with Gaussian noise of 10mV RMS and a BER of 10^{-20}. If you double the Gaussian noise to 20mV, what will the new BER be?

BER = exp(-sq(Vsnr)/2) = 1e-20. => Vsnr = 9.6 => Vsnr(new) = 9.6/2 = 4.8.

➔ BER = exp(-sq(Vsnr(new))/2) =1e-5.

B. In a signaling system where the line is terminated at both ends into a matched impedance, what is the percentage of ISI caused by a 10% terminator mismatch at both ends?

*10% mismatch causes reflection coefficient of 5%. So, for terminator mismatch at both ends, you need to have two termination bounces to cause ISI. So you will have 5%*5%=0.25% ISI at the receiver. Remember that ISI means "intersymbol interference"-- One symbol will degrade the noise margins for another symbol later on in time. This does not include the 5% degradation in the present bit, due to terminator mismatch.*

A brute force synchronizer uses a flip-flop with an aperture time of 100ps and a regeneration time constant of 100ps driven by a 1GHz clock. The synchronizer currently uses a waiting time, t_w, that gives a failure rate of 10^{-10}. If you double this waiting time, what will the new failure rate be? (Above should say "failure probability")

*From book p. 469, Probability of Failure = ta*fa*exp(-tw / Taus) = 1e-10.*

where ta=aperture time, fa=frequency of synchronizer, taus=regeneration time

➔ failure rate is exponentially dependent on waiting time. => tw=2.07ns for failure rate=1e-10. Let tw=4.14ns. Then, failure rate = 1e-19.

C. A system employs synchronous timing and stacks three bits on the transmission line between two modules. What should the relationship be between the delay of the transmission line and the bit time to center the clock on the eye? (For the purposes of this problem, assume zero t_{dCQ} and zero rise/fall time.)

From book p. 399, tr=0 and tdcq=0, essentially no aperture time. So, using equation 9-2,

$$\frac{tu+twire}{N} \le tbit \le \frac{twire - tu}{N-1}$$

Assuming tu=0, this becomes: $\frac{twire}{3} \le tbit \le \frac{twire}{2}$ *➔ tbit = twire/2.5.*

This also will be the case when the length of the line is always a certain number of integers plus 1/2 tbit, so that there are you always sample at the the end of the line exactly in the center of the eye.

D. To avoid dropping or duplicating symbols, when is a plesiochronous FIFO synchronizer allowed to adjust its read pointer?

When there is a "null" symbol in the register, you can either drop the null symbol or duplicate one.

A two-register plesiochronous synchronizer moves a signal between two 100MHz +/- 100ppm clock domains. What is the minimum frequency at which the synchronizer register selection must be updated?

Worst case is if the first clock is slow by 100MHz – 100ppm, and the second clock is fast by 100MHz + 100ppm. So, the maximum frequency difference between two clocks is 200ppm, or 20kHz. That is the point where you will lose a bit due to frequency drift. The pointers must be updated at a frequency of at least 20kHz or they will slip through a bit time.

E. A pipelined timing system operates at the maximum possible rate of 1Gb/s over a 10ns line. If the length of the line is doubled while all other parameters (rise-time, aperture, skew, and jitter) remain constant, what is the new maximum signaling rate? (Assume that attenuation of the longer line is not a factor.)

Assume trise+taperture+tuncertainty=1ns. Regardless of whether the line is doubled or not, we are limited by the process, and our ability to switch bits onto the line. Therefore, the maximum signaling rate will be 1Gb/s, regardless of increasing the length of the line, since we can't send bits onto the line faster than 1Gb/s.

F. If the peak-to-peak timing uncertainty in the system of problem (G) is doubled from 300ps to 600ps what happens to the maximum signaling rate?

If tu is increased from 300ps → 600ps, than our minimum bit time increases from 1ns → 1.3ns. In this case, the maximum speed we can switch bits will be 1/1.3ns = 770MHz.

G. On chip clock distribution is easier than off chip clock distribution because the on-chip wires are of much higher quality (true or false)?

False, on chip clock disctribution is hard because you cannot treat on chip lines as tranmission lines, since RC dominates on chip. So, can't take advantage of the wave effect of tranmission lines, and therefore have slow rise times due to big RC's.

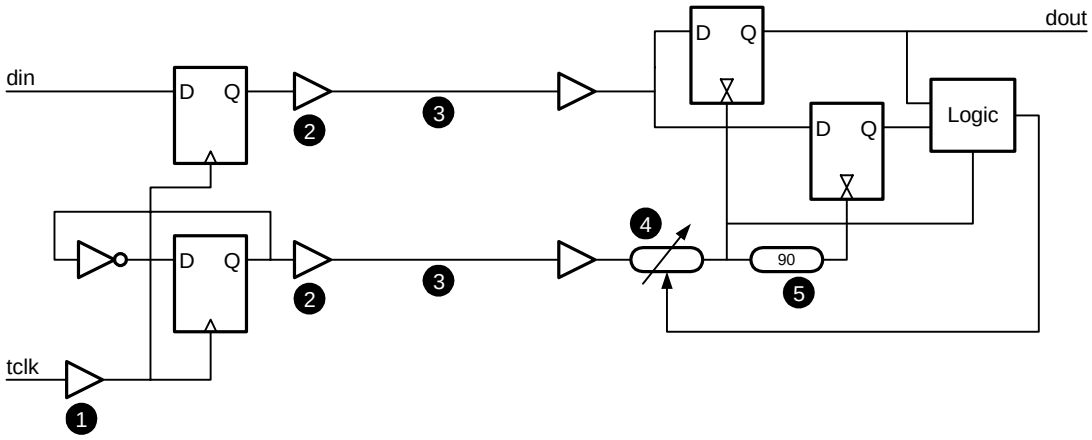
H. A brute force synchronizer has a failure probability of 10^{-30}. If the aperture time of a flip-flop used as the first stage of a brute force synchronizer is doubled while all other parameters (including the regeneration time constant of the flip-flop) are held constant, what will the new failure probability be?

From part(c), Probability of Failure = $ta*fa*\exp(\frac{-tw}{Taus})$.

Since aperture time is the only thing changing, the failure rate increases linearly by a factor of 2 greater.

→ *2*1e-30=2e-30.*

Problem 4: Timing [24 points total]



The figure above illustrates a 1Gb/s closed loop timing system with five sources of delay, skew, and jitter identified by white numbers in black circles. The sources are:

No	Description	Delay	Skew	Jitter (p-p)
1	Transmit clock buffer tree	2000ps	N/A	200ps
2	Transmit flip flops and drivers	500ps	25ps	50ps
3	Transmission line	2000ps	200ps	0ps
4	Variable delay	100-600ps	N/A	10%
5	Fixed 90-degree delay	500ps	50ps	50ps

Note that skew for a single element (like 5) refers to variation from nominal delay while skew for a pair of elements (2 and 3) refers to the difference between the two elements. Also note that skew is a magnitude (e.g., 50ps means +/- 50ps from the nominal value) and jitter is given as peak-to-peak.

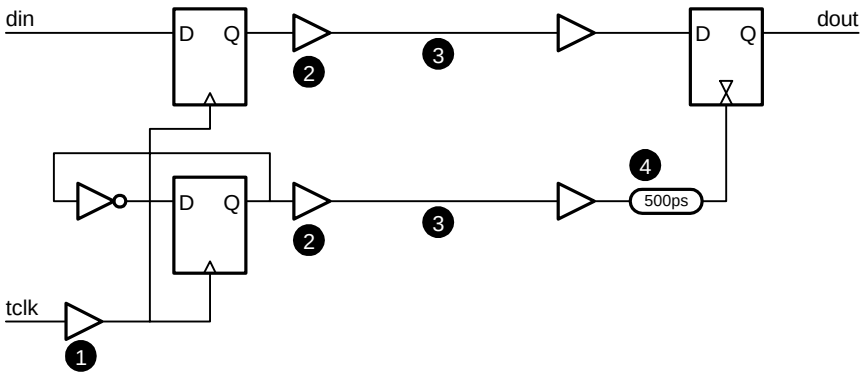
The system operates by using a 1GHz transmit clock, tclk, to clock both a data flip-flop (top) and a toggle flip-flop (bottom) that generates a 500MHz reference clock. Jitter in the transmit flip-flops is completely correlated. That is, if the delay of the upper flip-flop is increased by 25ps, the delay of the lower flip-flop is increased by the same amount. The data and reference clock are transmitted over parallel transmission lines that are matched to within 200ps. At the receiver the reference clock is delayed by a variable delay line to center it on the data eye and used to clock a double-edge-triggered flip-flop to recover the data. The clock is delayed by a further 90-degrees (to sample the edge) and used to clock another double-edge triggered flip-flop. A logic block (which may include additional flip-flops) uses the two data samples to control the variable delay line.

A. (8 points) Which of the skew and jitter sources listed above contribute to the overall uncertainty of the timing system? That is, which are not compensated by the design of the system? Circle the contributing elements in the table below:

No	Description	Delay	Skew	Jitter
1	Transmit clock buffer tree	2000ps	N/A	~~200ps~~
2	Transmit flip flops and drivers	500ps	~~25ps~~	50ps
3	Transmission line	2000ps	~~200ps~~	0ps
4	Variable delay	100-600ps	N/A	10%
5	Fixed 90-degree delay	500ps	50ps	50ps

Any skew occurring on the lines or between the flip flops/drivers are cancelled, since this fixed offset is compensated for adjusting the receive side flip flop clock based upon the per line closed loop timing. The jitter from the transmit clock buffer tree is also cancelled since any jitter in the data will also be seen in the clock that is being transmitted along with the data.

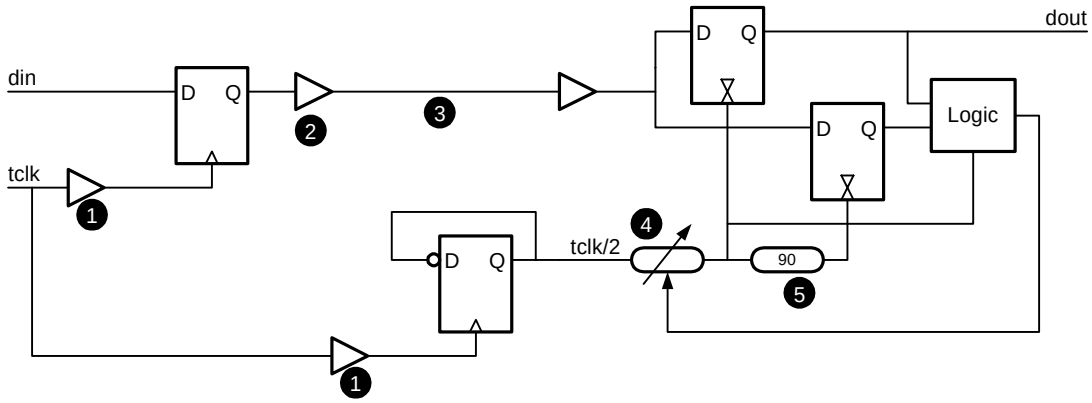
B. (8 points) Consider the revised system below where the variable delay line is replaced by a fixed 500ps delay. How does this change how the five elements above contribute to timing uncertainty. List the elements that change:



In this one, we no longer are sampling our data twice, both in phase and 90 degrees from that, in order to compensate for skew. Instead, we assume that both lines have very little skew, such that we can clock to data exactly in the center of the eye. In this sense, we now see the skew of the tranmission line, and the transmit flip flops and drivers. The only thing we will have cancelled would be the jitter of the transmit clock buffer tree.

Transmit flip flops and drivers	*25ps (skew)*
Transmission line	*200ps (skew)*

C. (8 points) Now consider returning to the original system (of part A) but replacing the reference clock by a mesochronous tclk/2 signal at the receiver. Compared to the system of part A, how does this change how the five elements above contribute to timing uncertainty. List the elements that change:



In this one, this is similar except for a few things. First, the jitter of the transmit clock buffer tree is included, since both paths have different amounts of jitter.(Since they have different clock buffers) Everything else will be exactly similar to part(A), as the skew from (2) and (3) will be compensated by the per pin closed loop timing.

Transmit clock buffer tree	*200ps (jitter)*